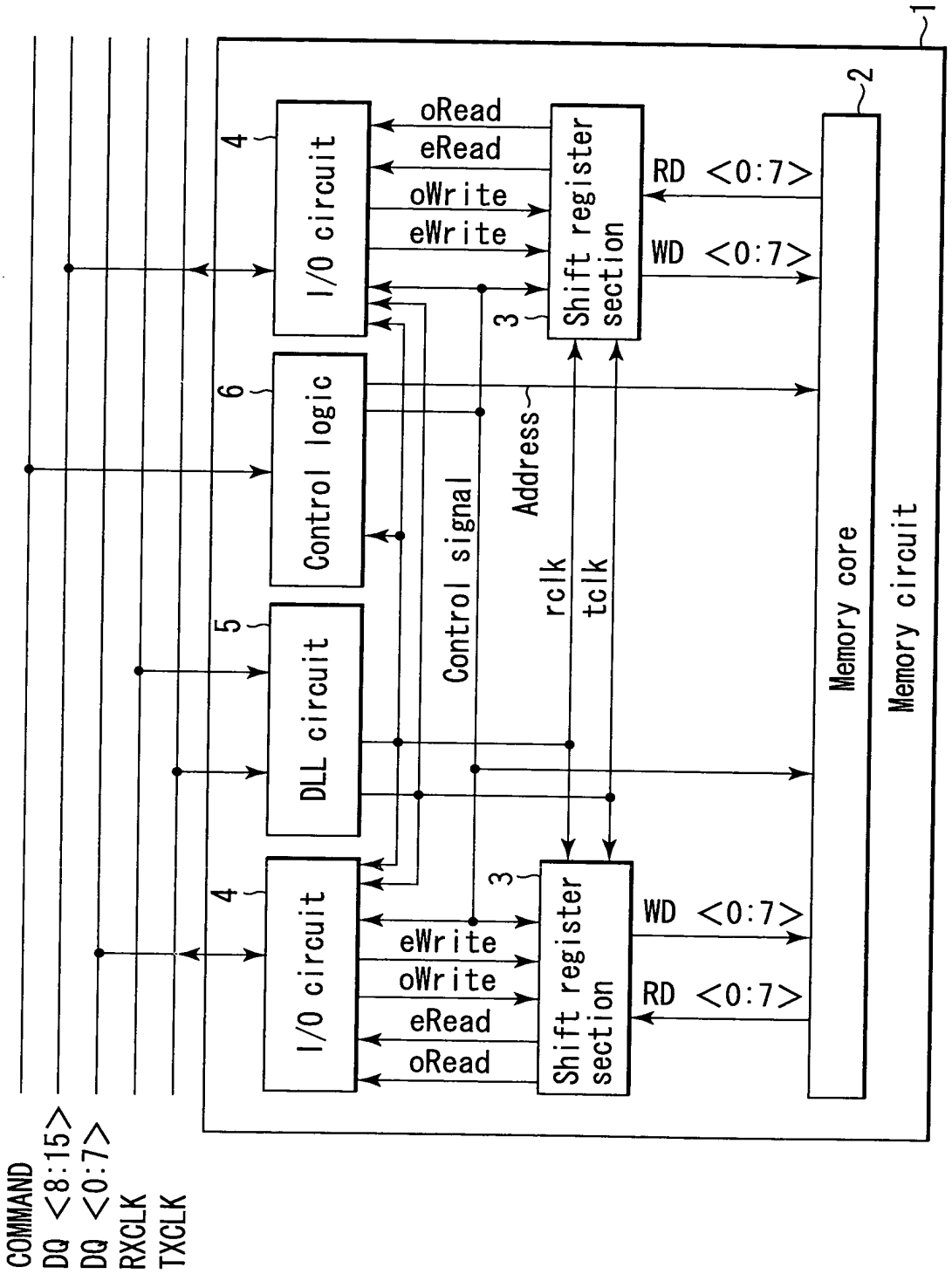

1
2
Memory circuit
Memory core
I/O circuit
4
oRead
eRead
oWrite
eWrite
Shift register section
3
RD <0:7>
WD <0:7>
Control logic
6
Address
Control signal
rclk
tclk
DLL circuit
5
COMMAND
DQ <8:15>
DQ <0:7>
RXCLK
TXCLK

FIG. 1

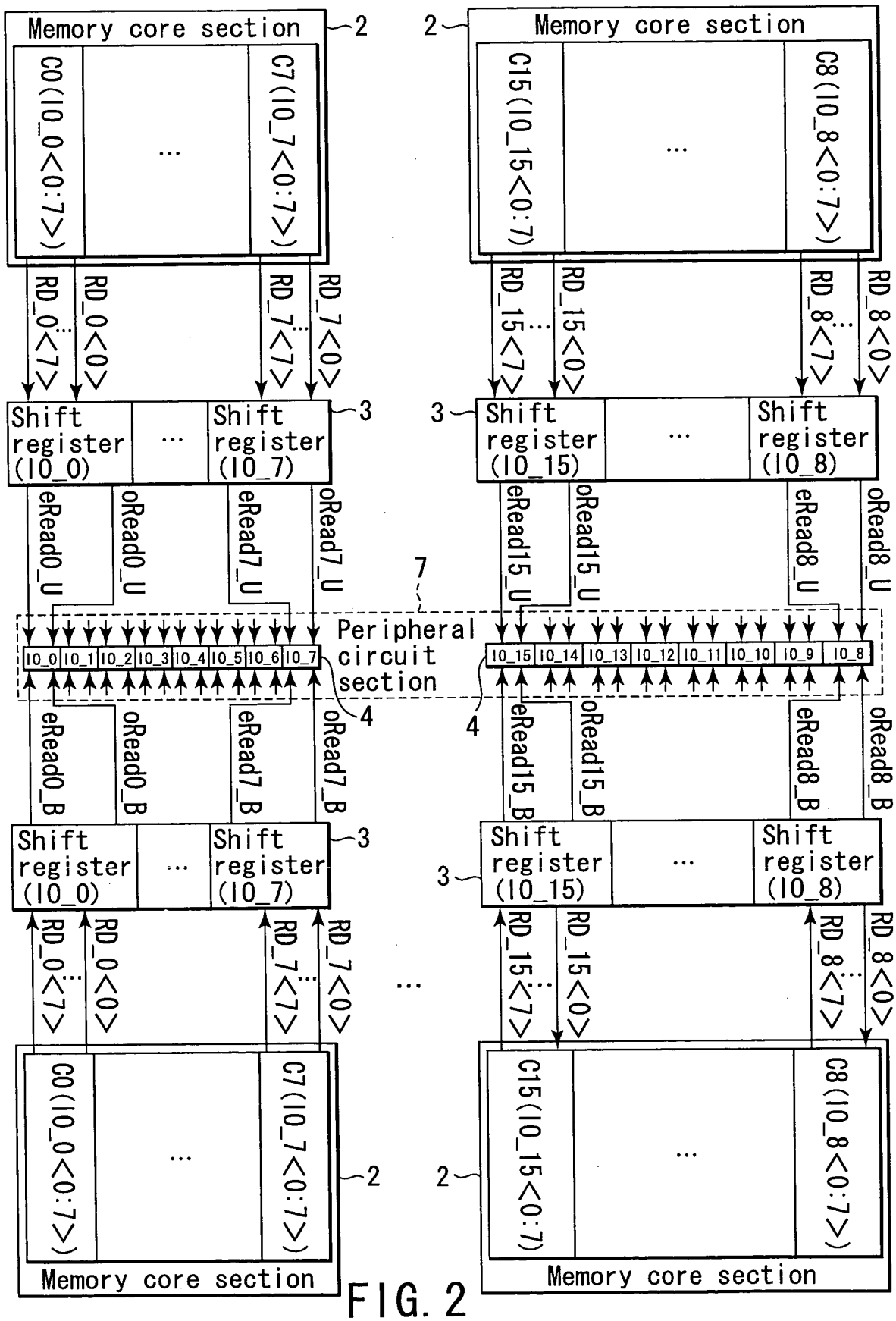

Memory core section
2
C0(IO_0<0:7>)
C7(IO_7<0:7>)
C15(IO_15<0:7)
C8(IO_8<0:7>)
RD_0<7>
RD_0<0>
RD_7<7>
RD_7<0>
RD_15<7>
RD_15<0>
RD_8<7>
RD_8<0>
Shift register (IO_0)
Shift register (IO_7)
Shift register (IO_15)
Shift register (IO_8)
3
eRead0_U
oRead0_U
eRead7_U
oRead7_U
eRead15_U
oRead15_U
eRead8_U
oRead8_U
7
Peripheral circuit section
IO_0 IO_1 IO_2 IO_3 IO_4 IO_5 IO_6 IO_7
IO_15 IO_14 IO_13 IO_12 IO_11 IO_10 IO_9 IO_8
4
eRead0_B
oRead0_B
eRead7_B
oRead7_B
eRead15_B
oRead15_B
eRead8_B
oRead8_B

FIG. 2

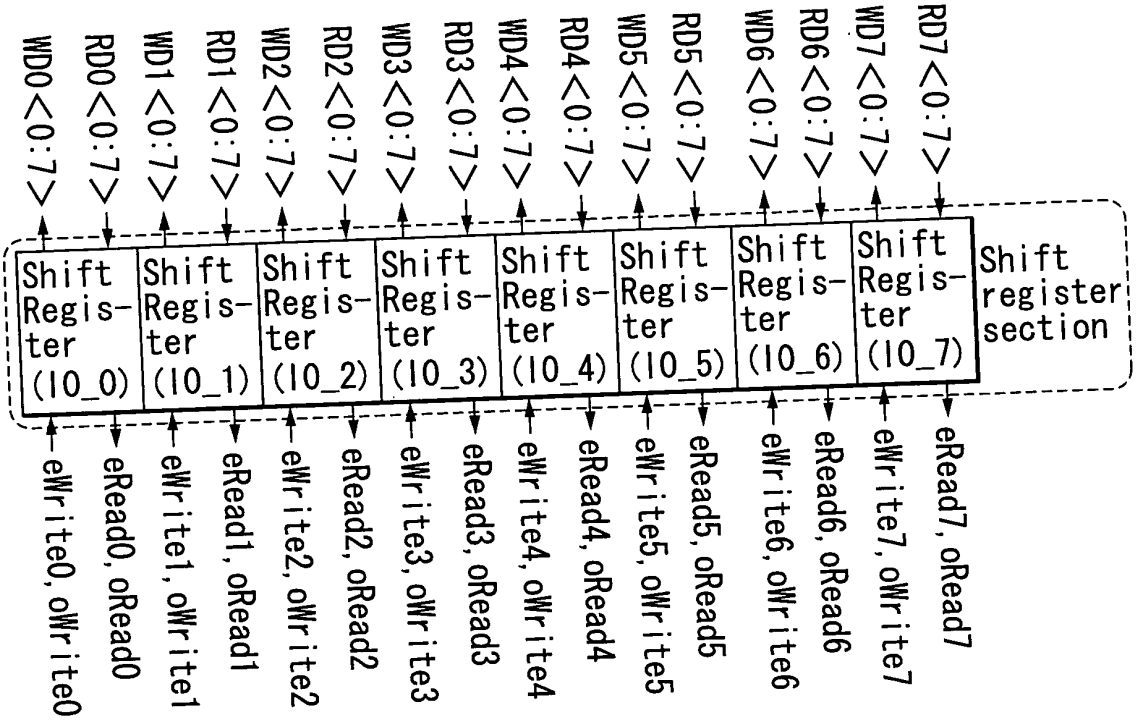

WD0<0:7>
RD0<0:7>
WD1<0:7>
RD1<0:7>
WD2<0:7>
RD2<0:7>
WD3<0:7>
RD3<0:7>
WD4<0:7>
RD4<0:7>
WD5<0:7>
RD5<0:7>
WD6<0:7>
RD6<0:7>
WD7<0:7>
RD7<0:7>
Shift Register (IO_0)
Shift Register (IO_1)
Shift Register (IO_2)
Shift Register (IO_3)
Shift Register (IO_4)
Shift Register (IO_5)
Shift Register (IO_6)
Shift Register (IO_7)
Shift register section
eWrite0, oWrite0
eRead0, oRead0
eWrite1, oWrite1
eRead1, oRead1
eWrite2, oWrite2
eRead2, oRead2
eWrite3, oWrite3
eRead3, oRead3
eWrite4, oWrite4
eRead4, oRead4
eWrite5, oWrite5
eRead5, oRead5
eWrite6, oWrite6
eRead6, oRead6
eWrite7, oWrite7
eRead7, oRead7

FIG. 3A

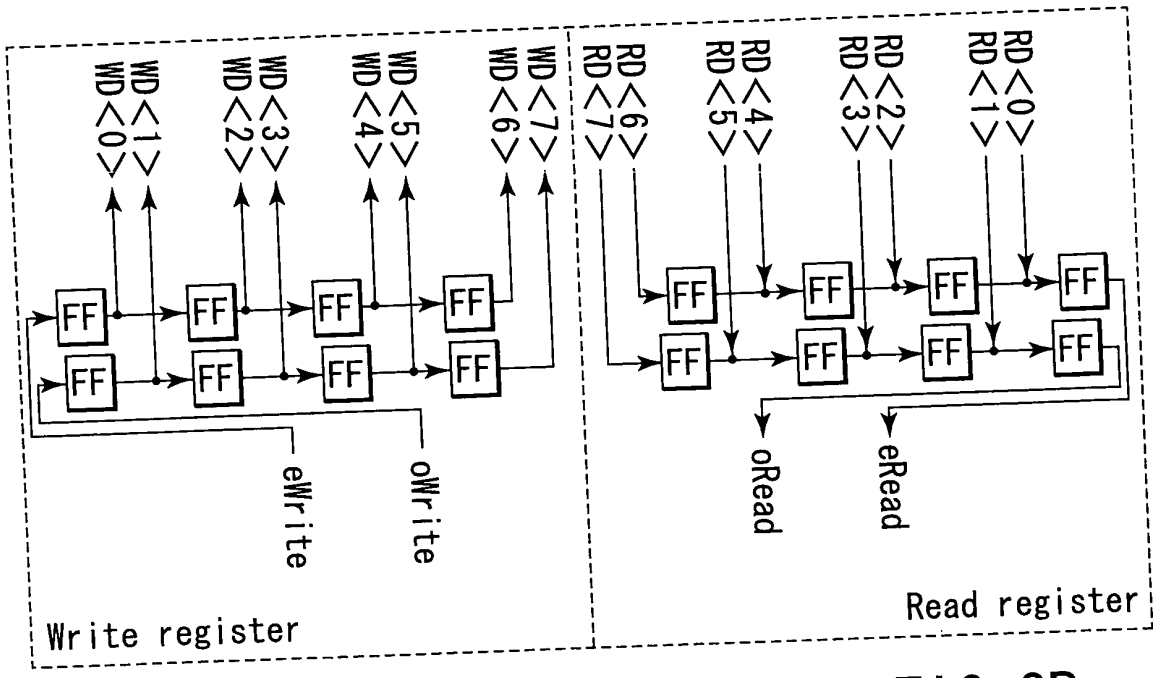

WD<0>
WD<1>
WD<2>
WD<3>
WD<4>
WD<5>
WD<6>
WD<7>
FF
eWrite
oWrite
Write register
RD<7>
RD<6>
RD<5>
RD<4>
RD<3>
RD<2>
RD<1>
RD<0>
oRead
eRead
Read register

FIG. 3B

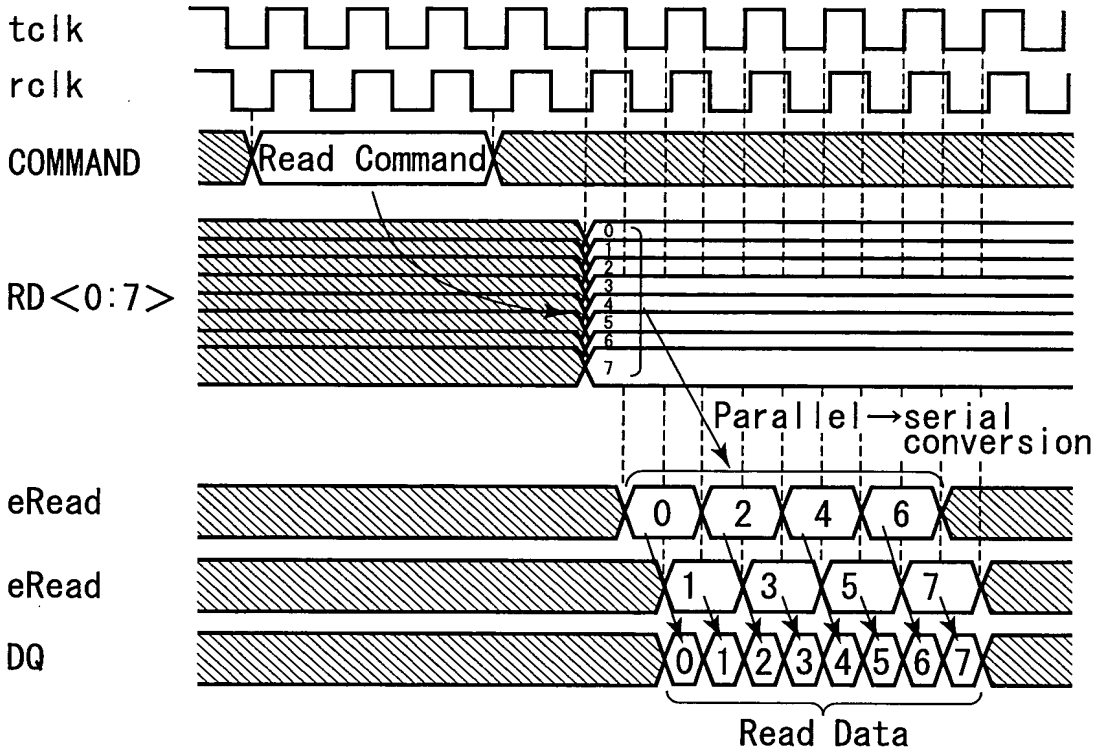

tclk
rclk
COMMAND
Read Command
RD<0:7>
0
1
2
3
4
5
6
7
Parallel→serial conversion
eRead
0 2 4 6
eRead
1 3 5 7
DQ
0 1 2 3 4 5 6 7
Read Data

FIG. 4

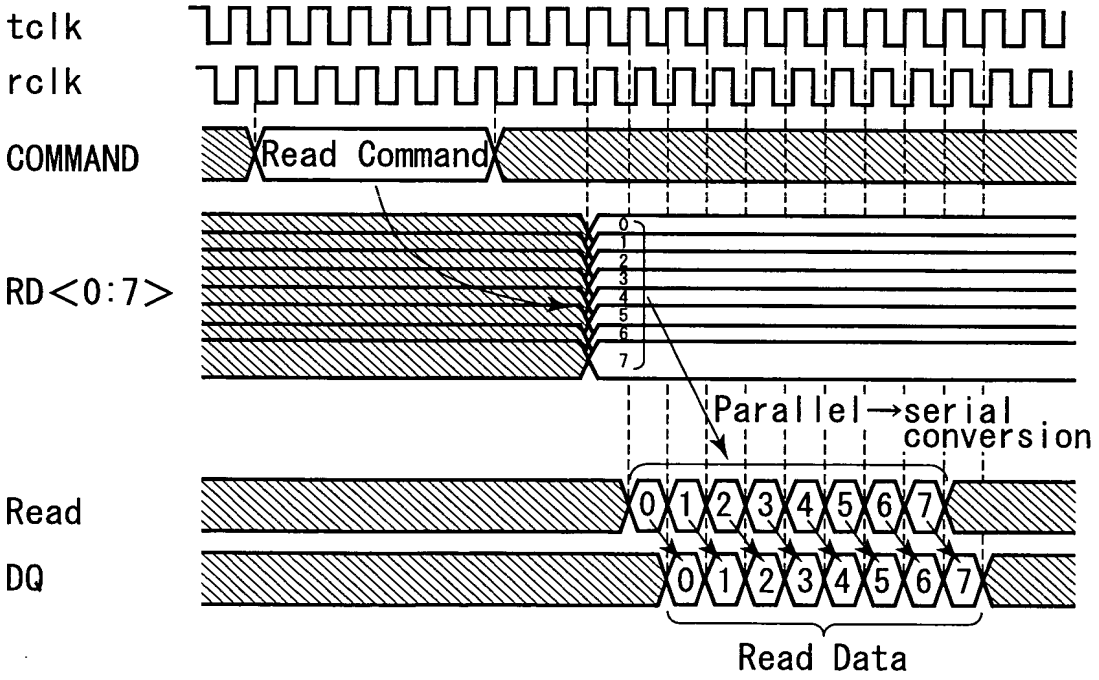

tclk
rclk
COMMAND
Read Command
RD<0:7>
0
1
2
3
4
5
6
7
Parallel→serial conversion
Read
0 1 2 3 4 5 6 7
DQ
0 1 2 3 4 5 6 7
Read Data

FIG. 5

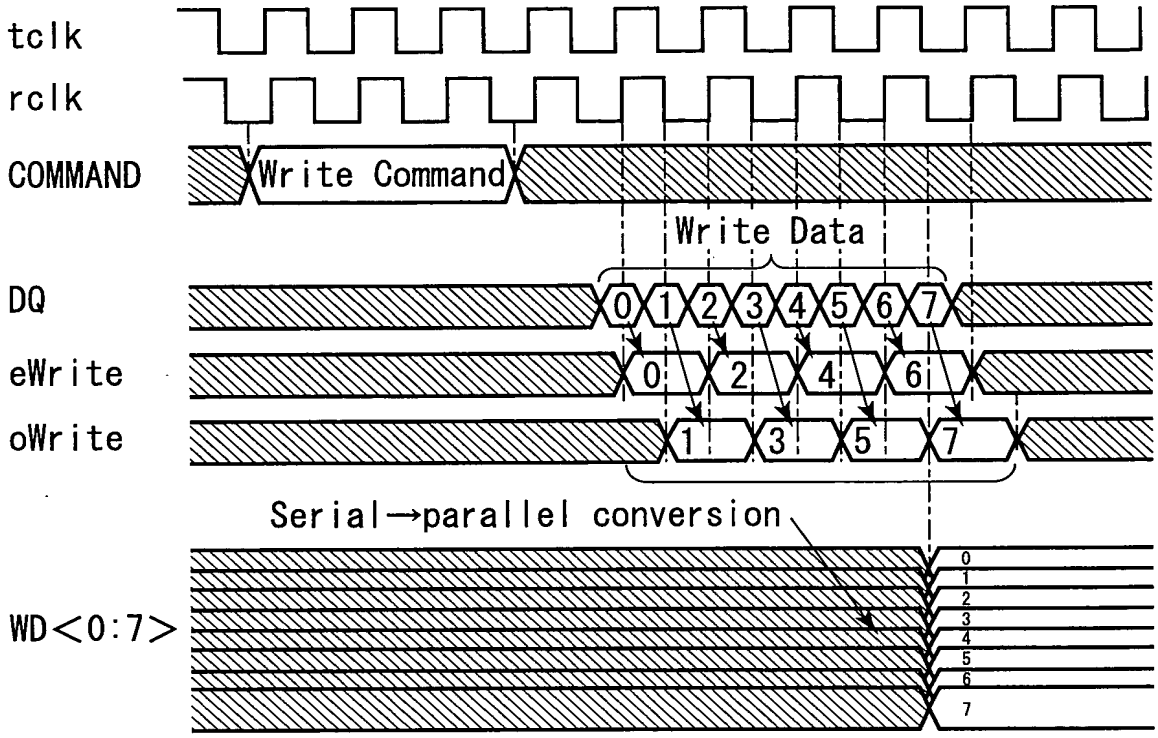

tclk
rclk
COMMAND
Write Command
Write Data
DQ
0 1 2 3 4 5 6 7
eWrite
0 2 4 6
oWrite
1 3 5 7
Serial→parallel conversion
WD<0:7>
0
1
2
3
4
5
6
7

FIG. 6

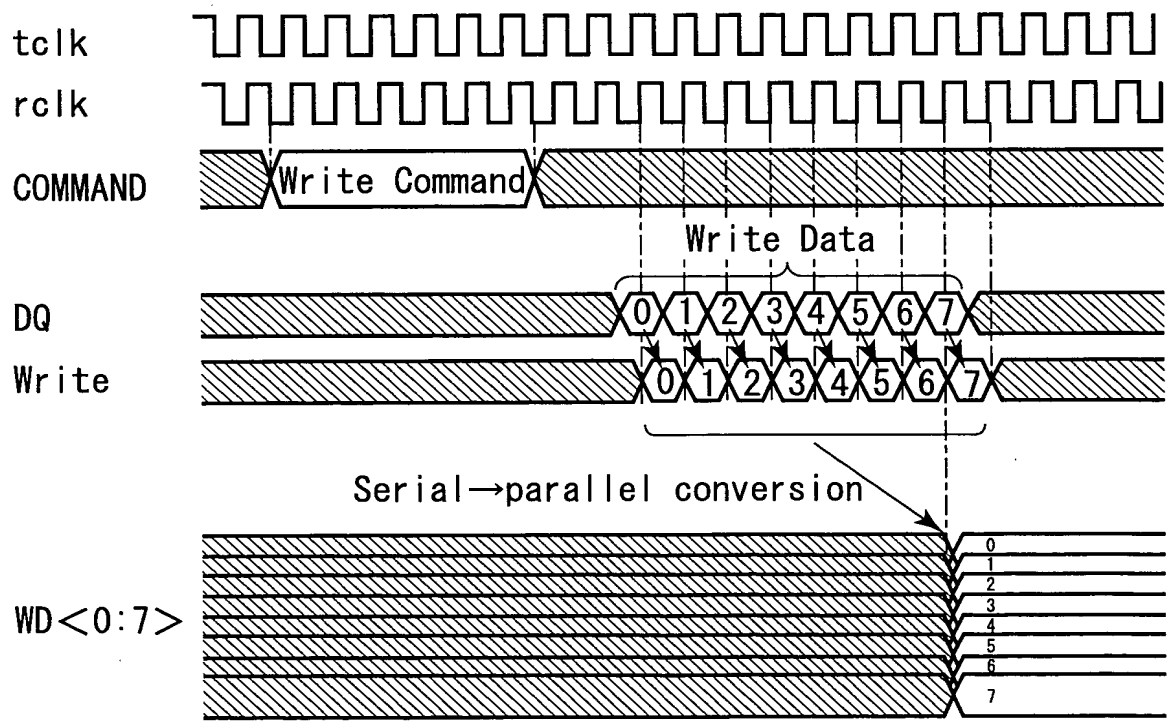

tclk
rclk
COMMAND
Write Command
Write Data
DQ
0 1 2 3 4 5 6 7
Write
0 1 2 3 4 5 6 7
Serial→parallel conversion
WD<0:7>
0
1
2
3
4
5
6
7

FIG. 7

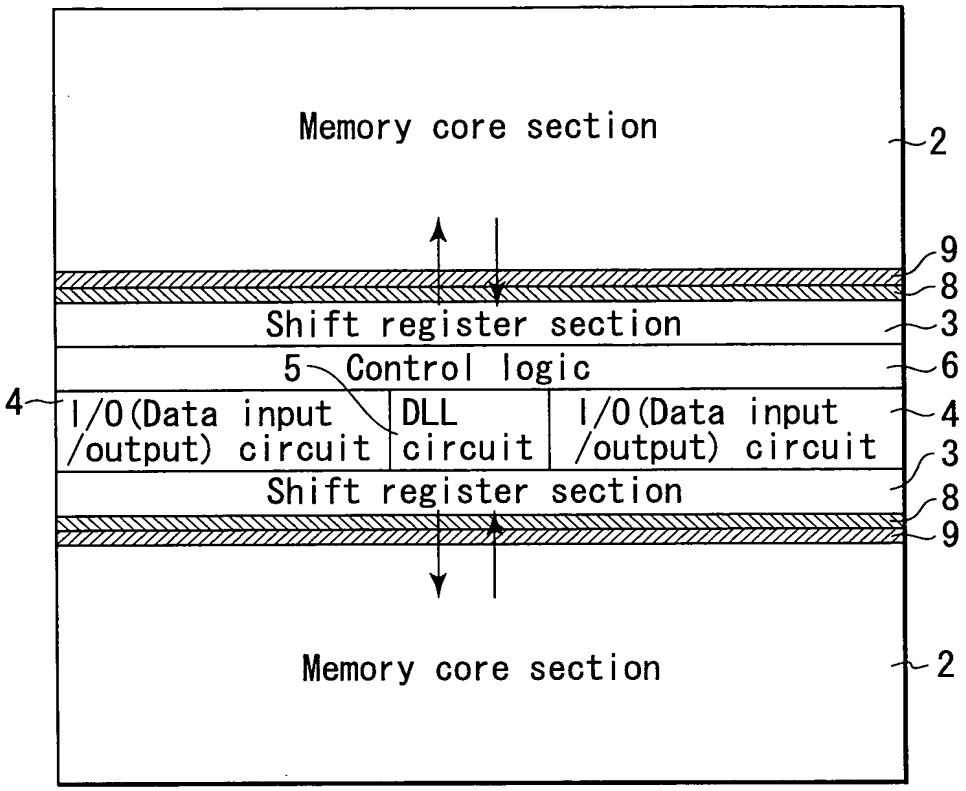

Memory core section
2
9
8
Shift register section
3
5
Control logic
6
4
I/O(Data input /output) circuit
DLL circuit
I/O(Data input /output) circuit
4
3
Shift register section
8
9
Memory core section
2

FIG. 8A

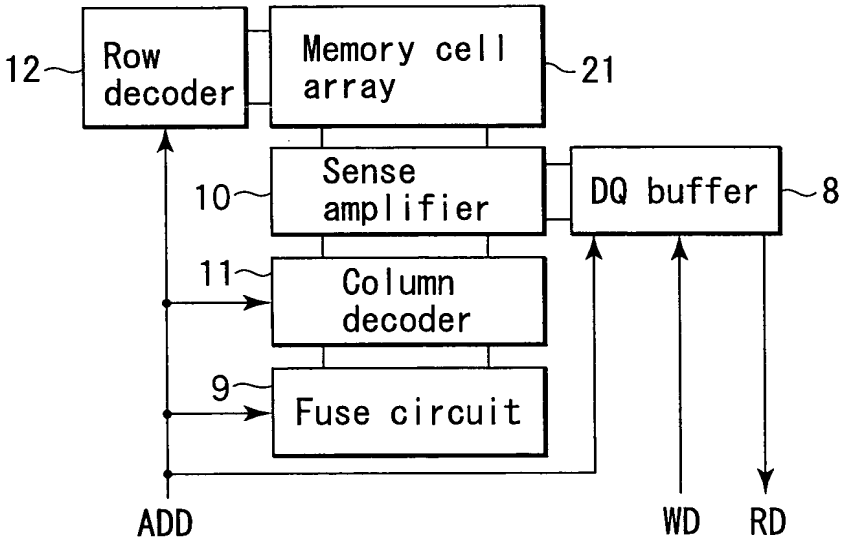

12
Row decoder
Memory cell array
21
10
Sense amplifier
DQ buffer
8
11
Column decoder
9
Fuse circuit
ADD
WD
RD

FIG. 8B

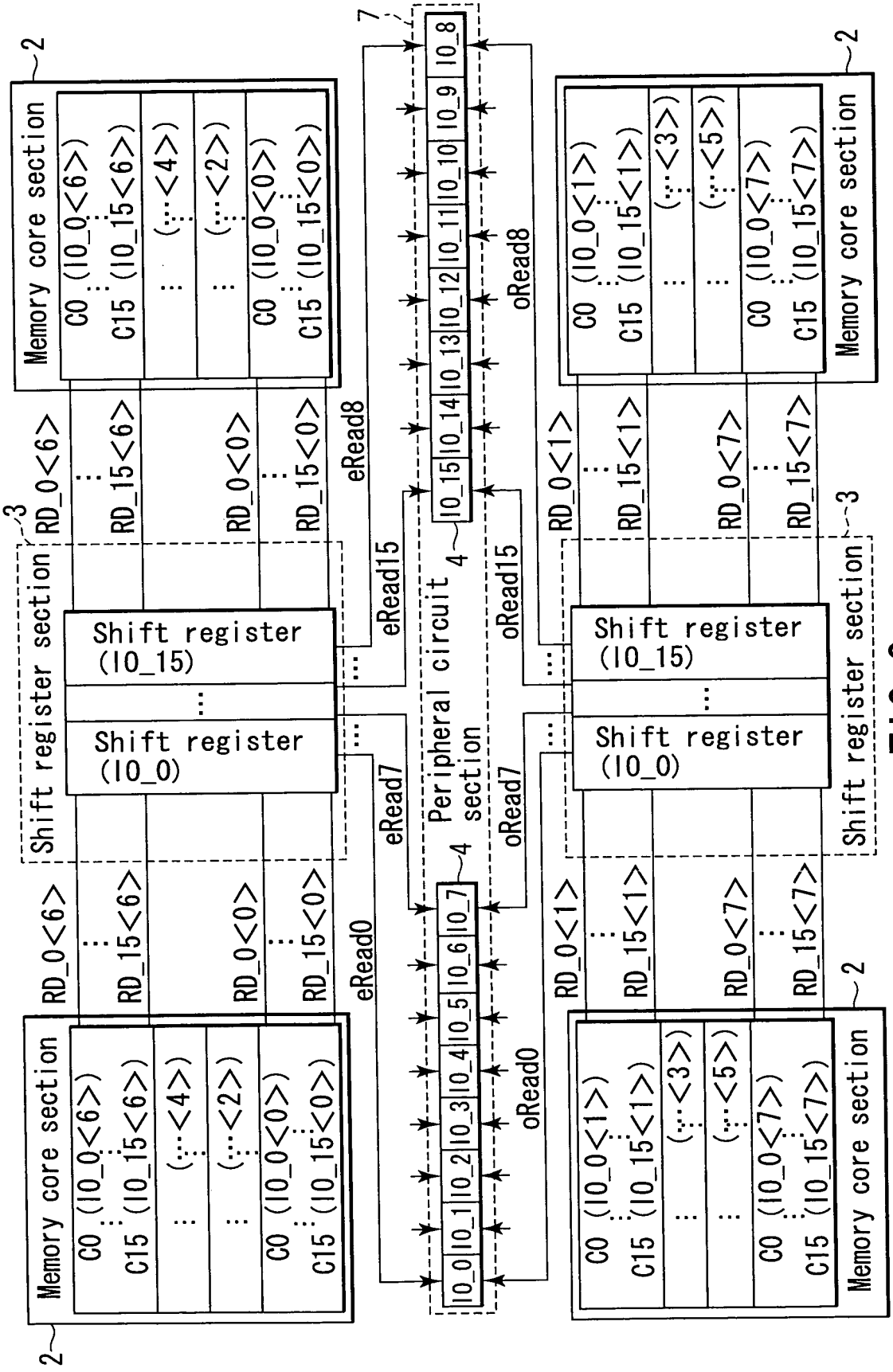

Memory core section
Shift register section
Shift register (IO_15)
Shift register (IO_0)
Peripheral circuit section
RD_0<6>
RD_15<6>
RD_0<0>
RD_15<0>
RD_0<1>
RD_15<1>
RD_0<7>
RD_15<7>
eRead0
eRead7
eRead8
eRead15
oRead0
oRead7
oRead8
oRead15
IO_0 IO_1 IO_2 IO_3 IO_4 IO_5 IO_6 IO_7
IO_8 IO_9 IO_10 IO_11 IO_12 IO_13 IO_14 IO_15
2
3
4
7

FIG. 9

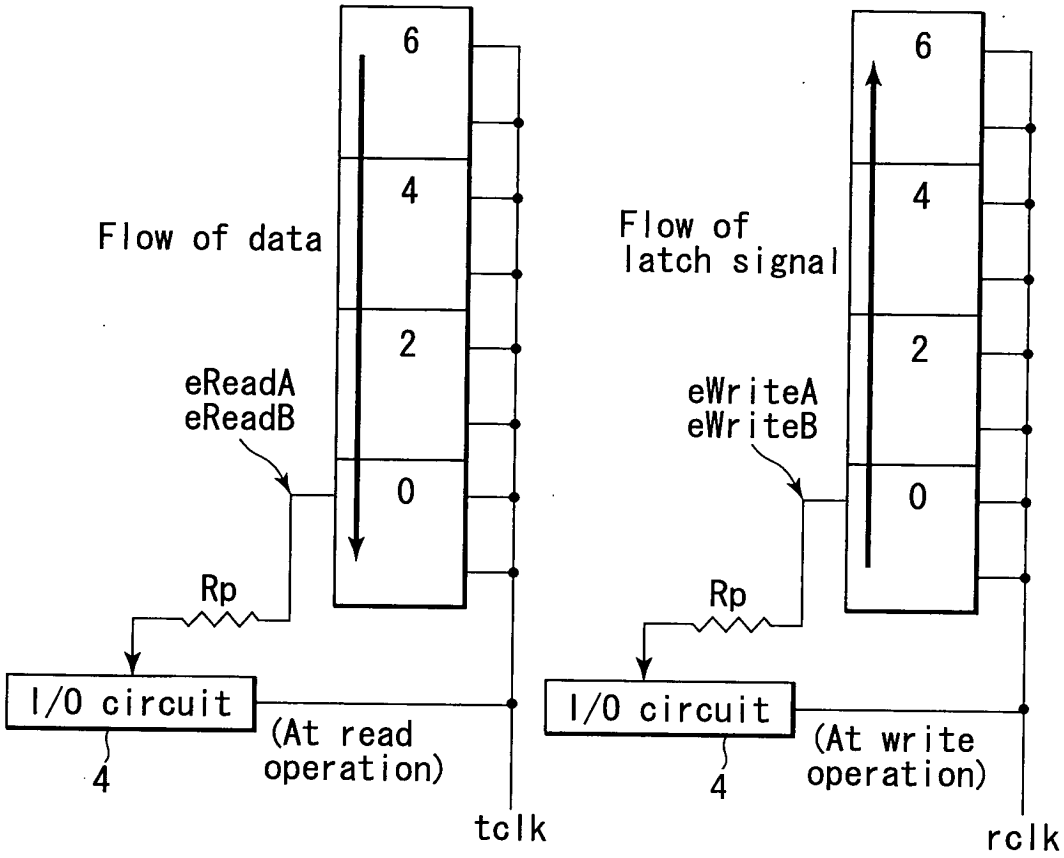


FIG. 10A

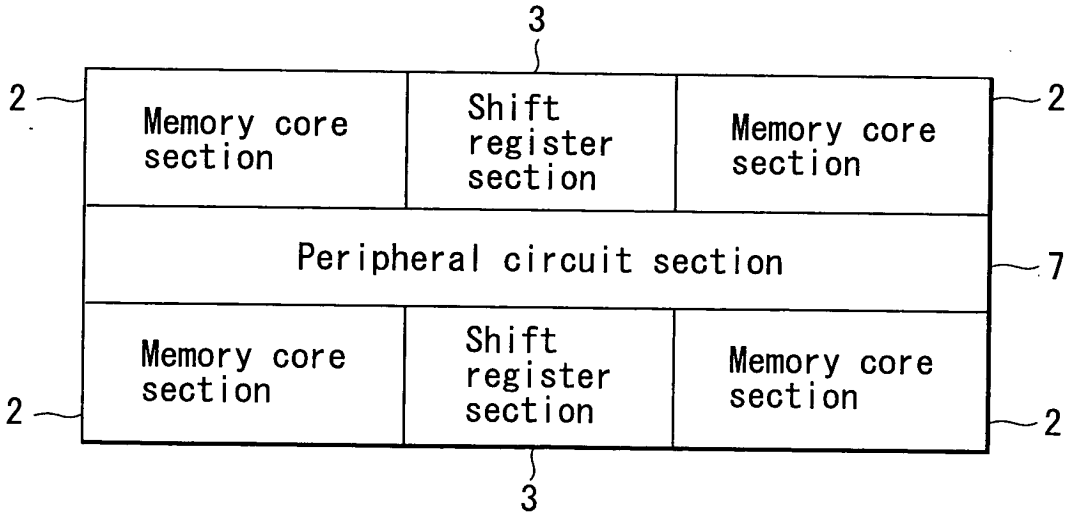


FIG. 10B

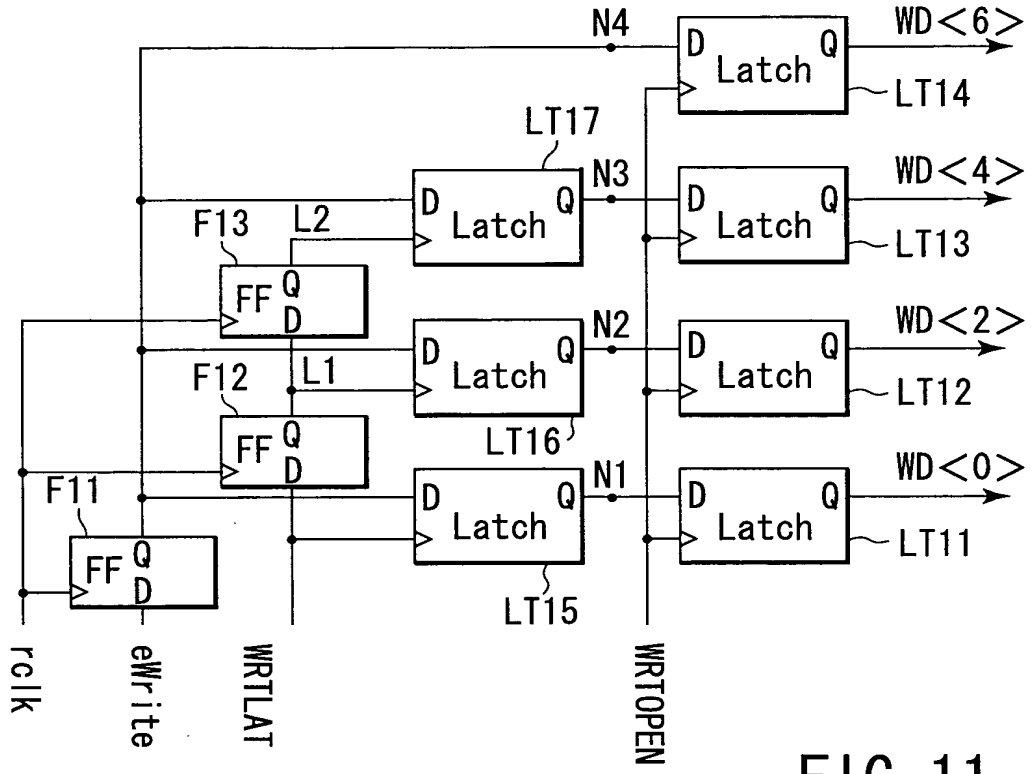

N4
WD<6>
D Latch Q
LT14
LT17
N3
WD<4>
F13
L2
LT13
FF Q D
N2
WD<2>
F12
L1
LT12
LT16
N1
WD<0>
F11
LT11
LT15
rclk
eWrite
WRTLAT
WRTOPEN

FIG. 11

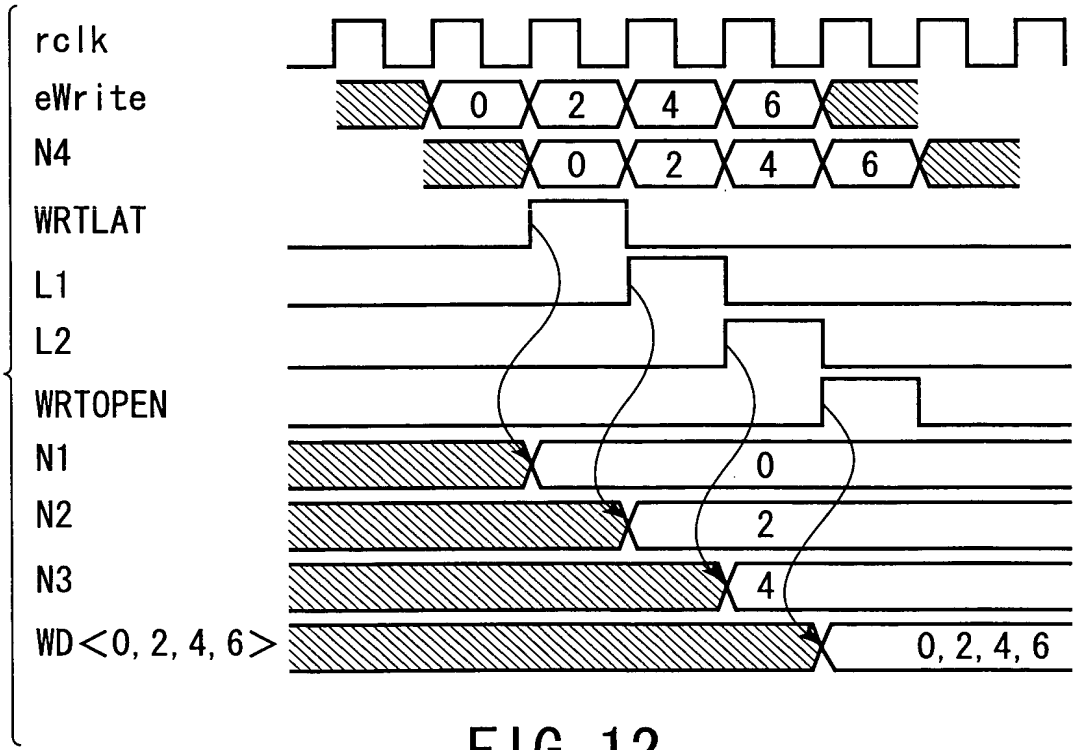

rclk
eWrite
0 2 4 6
N4
0 2 4 6
WRTLAT
L1
L2
WRTOPEN
N1
0
N2
2
N3
4
WD<0, 2, 4, 6>
0, 2, 4, 6

FIG. 12

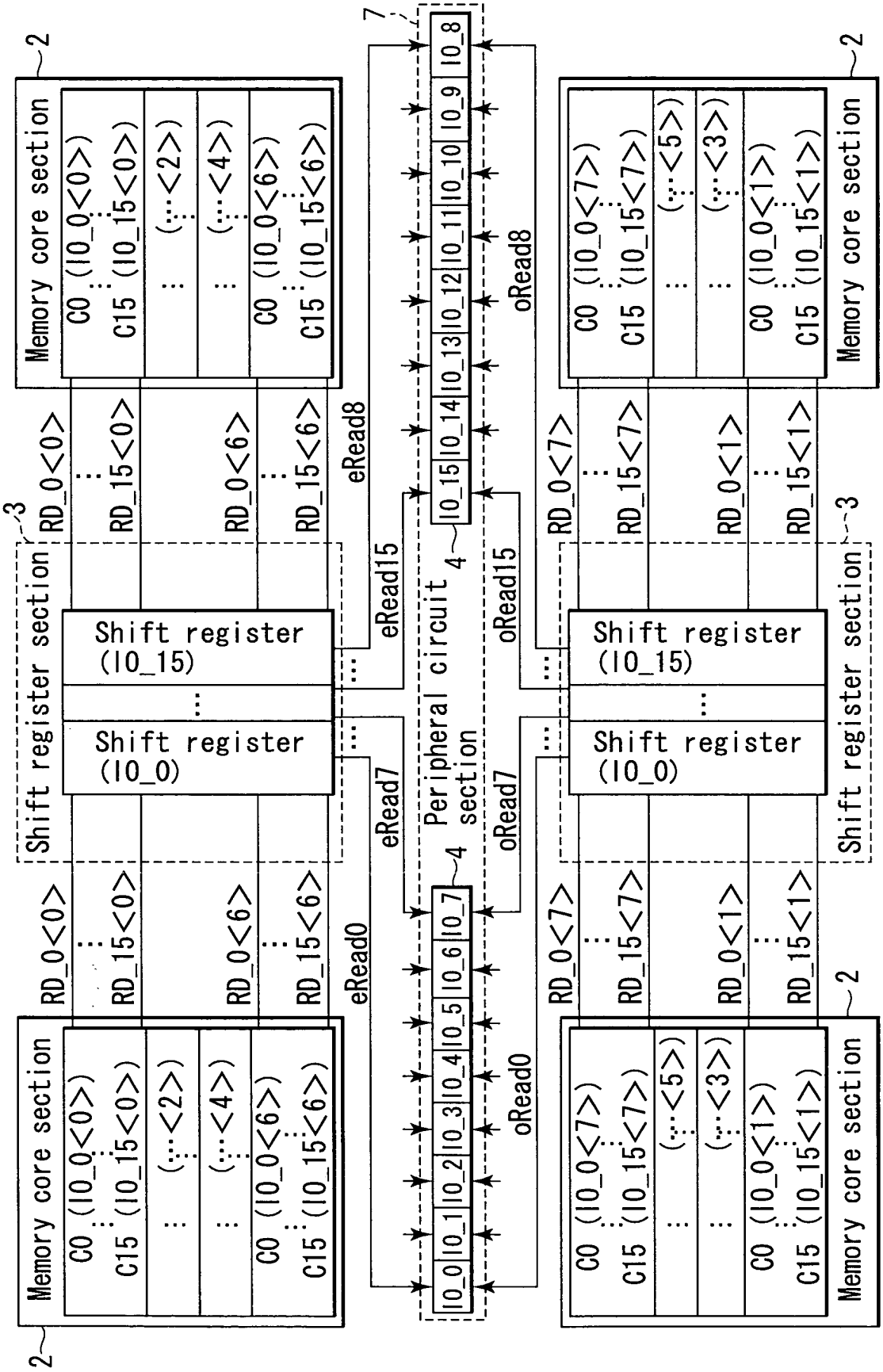

Memory core section
C0 (IO_0<0>)
C15 (IO_15<0>)
(...<2>)
(...<4>)
C0 (IO_0<6>)
C15 (IO_15<6>)
C0 (IO_0<7>)
C15 (IO_15<7>)
(...<5>)
(...<3>)
C0 (IO_0<1>)
C15 (IO_15<1>)
RD_0<0>
RD_15<0>
RD_0<6>
RD_15<6>
RD_0<7>
RD_15<7>
RD_0<1>
RD_15<1>
Shift register section
Shift register (IO_15)
Shift register (IO_0)
Peripheral circuit section
IO_0 IO_1 IO_2 IO_3 IO_4 IO_5 IO_6 IO_7
IO_8 IO_9 IO_10 IO_11 IO_12 IO_13 IO_14 IO_15
eRead0
eRead7
eRead8
eRead15
oRead0
oRead7
oRead8
oRead15
2
3
4
7

FIG. 13

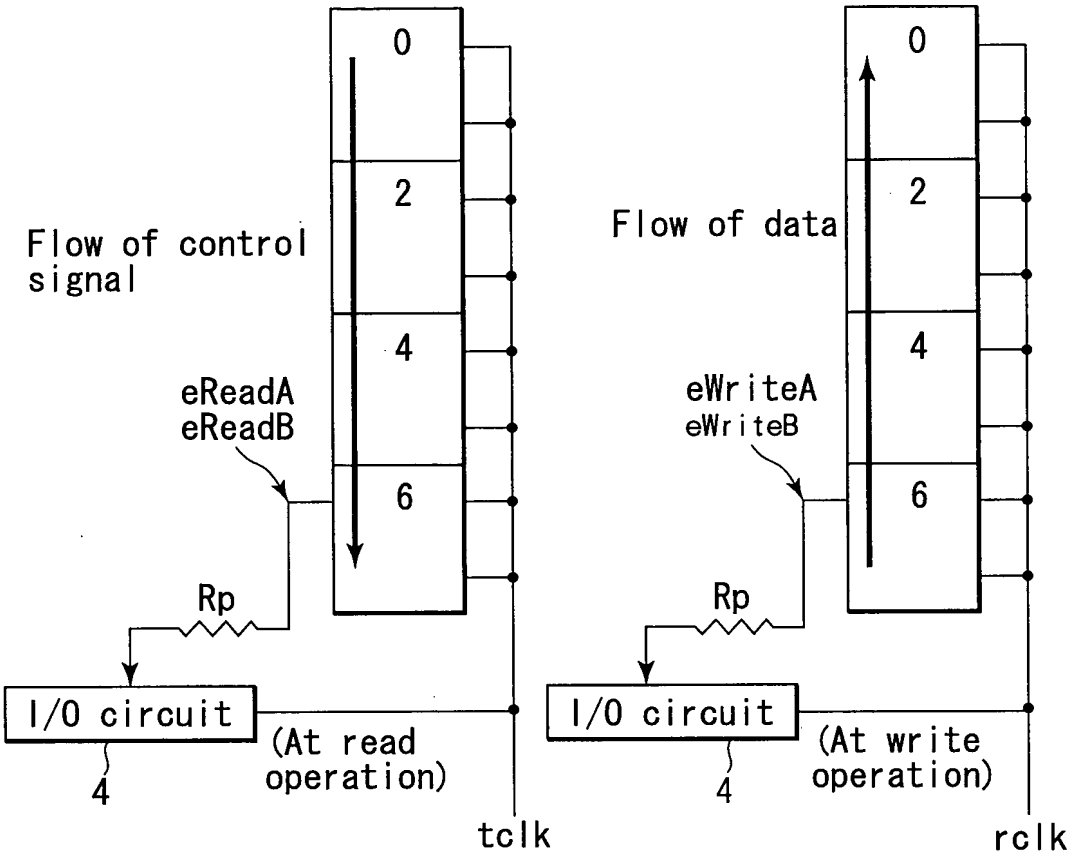


FIG. 14A

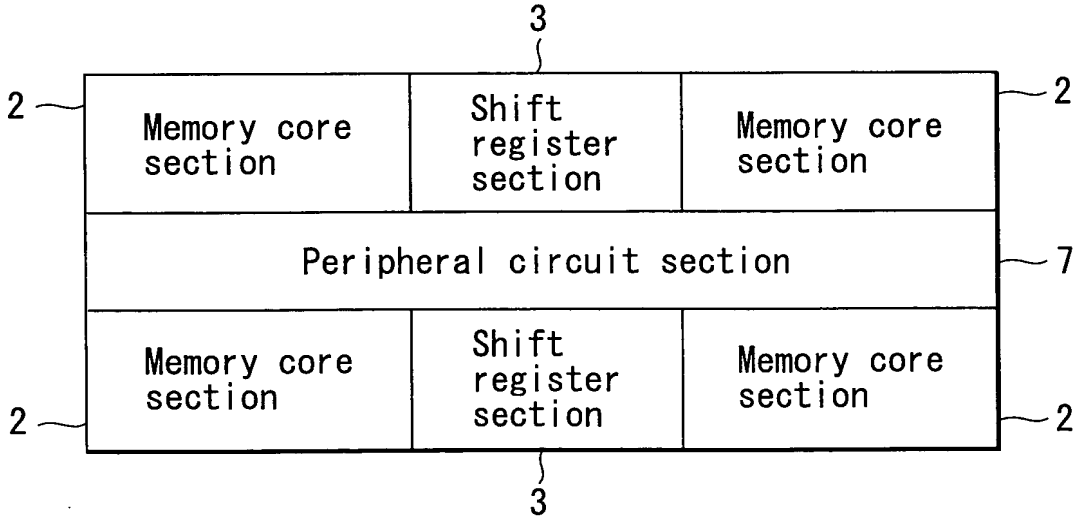


FIG. 14B

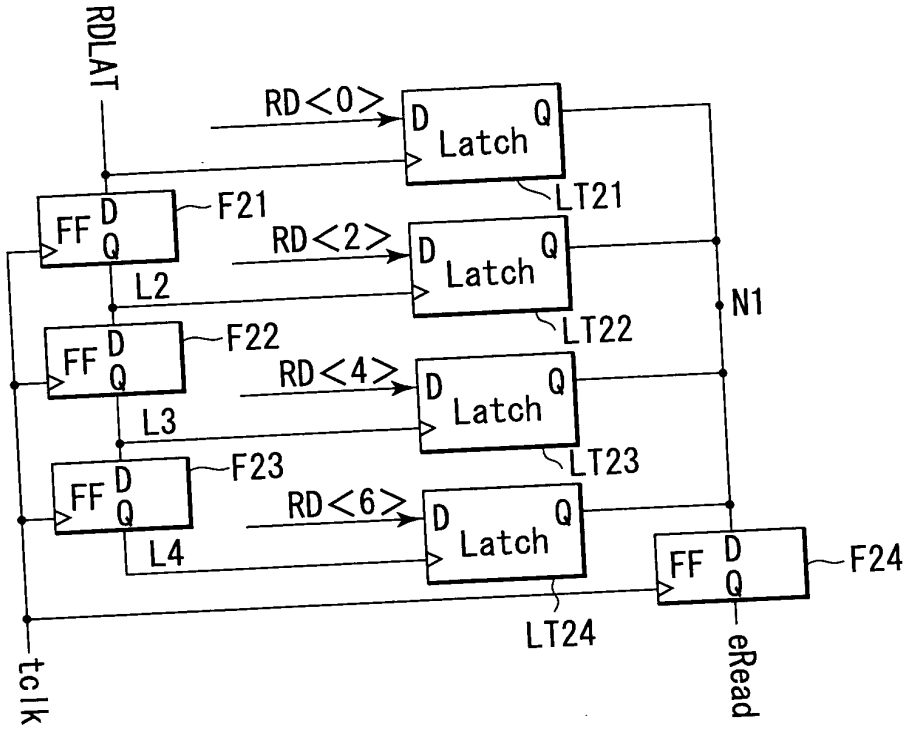

RDLAT
RD<0>
D Latch Q
LT21
FF D Q
F21
RD<2>
L2
N1
LT22
F22
RD<4>
L3
LT23
F23
RD<6>
L4
F24
LT24
tclk
eRead

FIG. 15

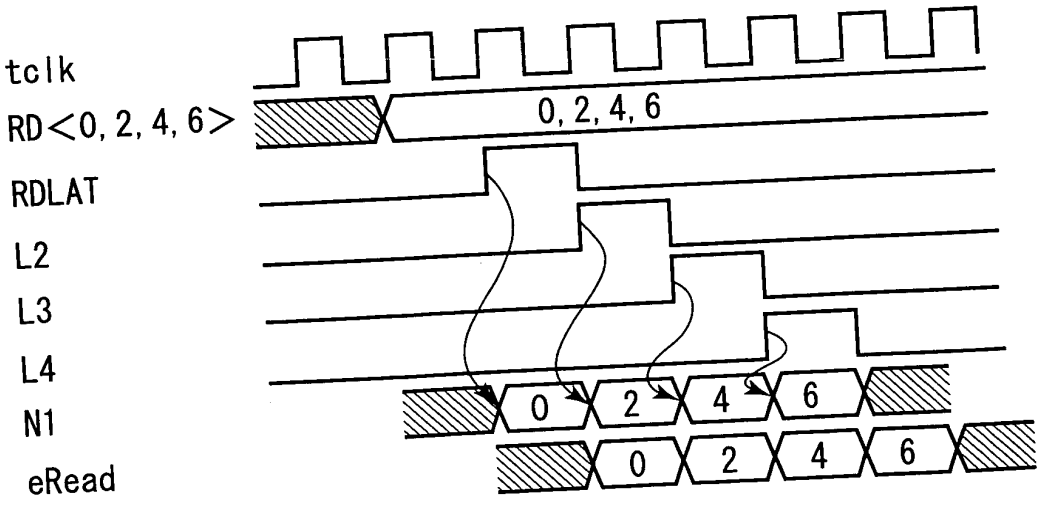

tclk
RD<0, 2, 4, 6>
0, 2, 4, 6
RDLAT
L2
L3
L4
N1
eRead
0
2
4
6
0
2
4
6

FIG. 16

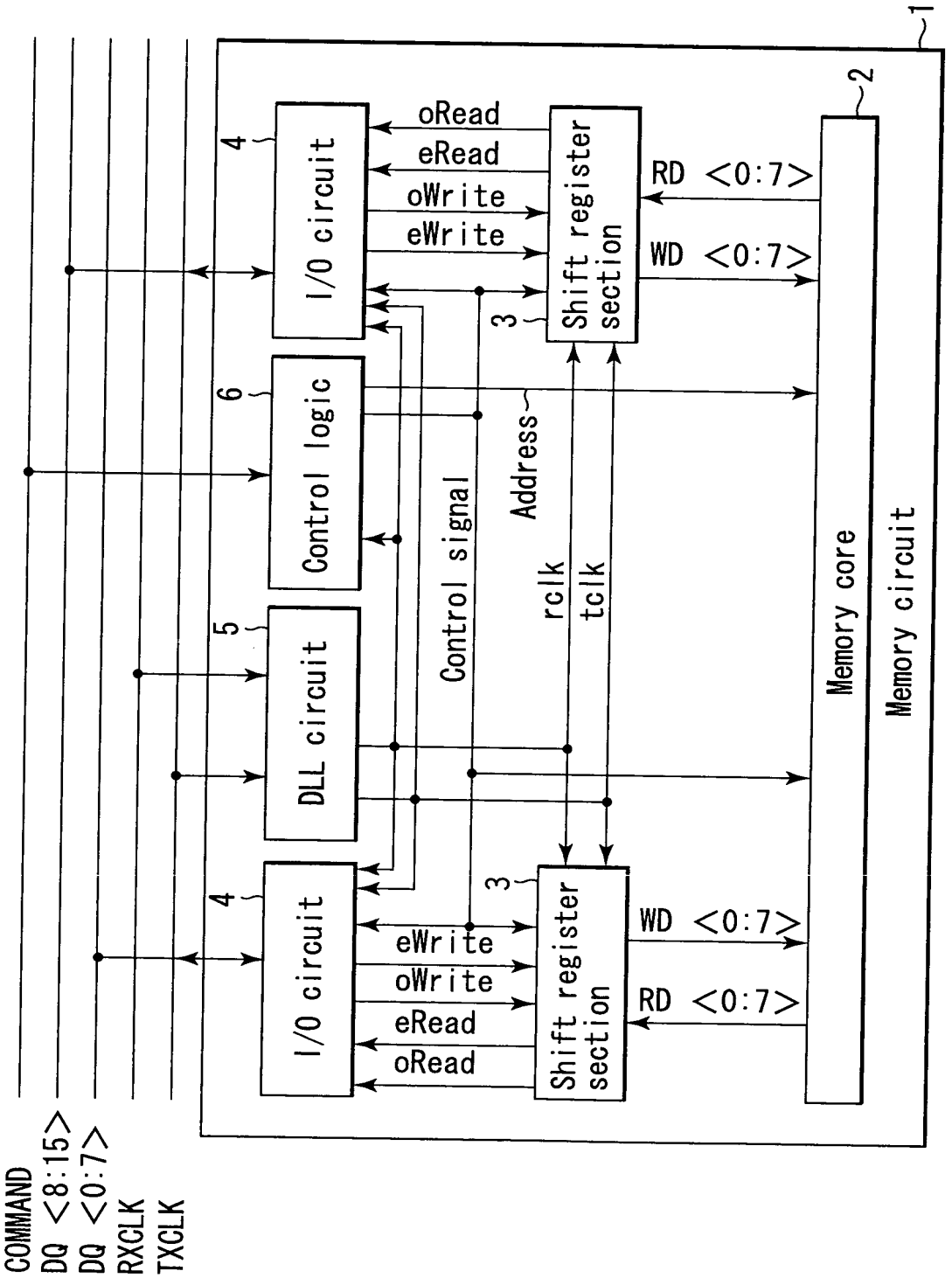

COMMAND
DQ <8:15>
DQ <0:7>
RXCLK
TXCLK
1
2
Memory circuit
Memory core
I/O circuit
4
oRead
eRead
oWrite
eWrite
Shift register section
3
RD <0:7>
WD <0:7>
Control logic
6
Address
Control signal
rclk
tclk
DLL circuit
5

FIG. 17

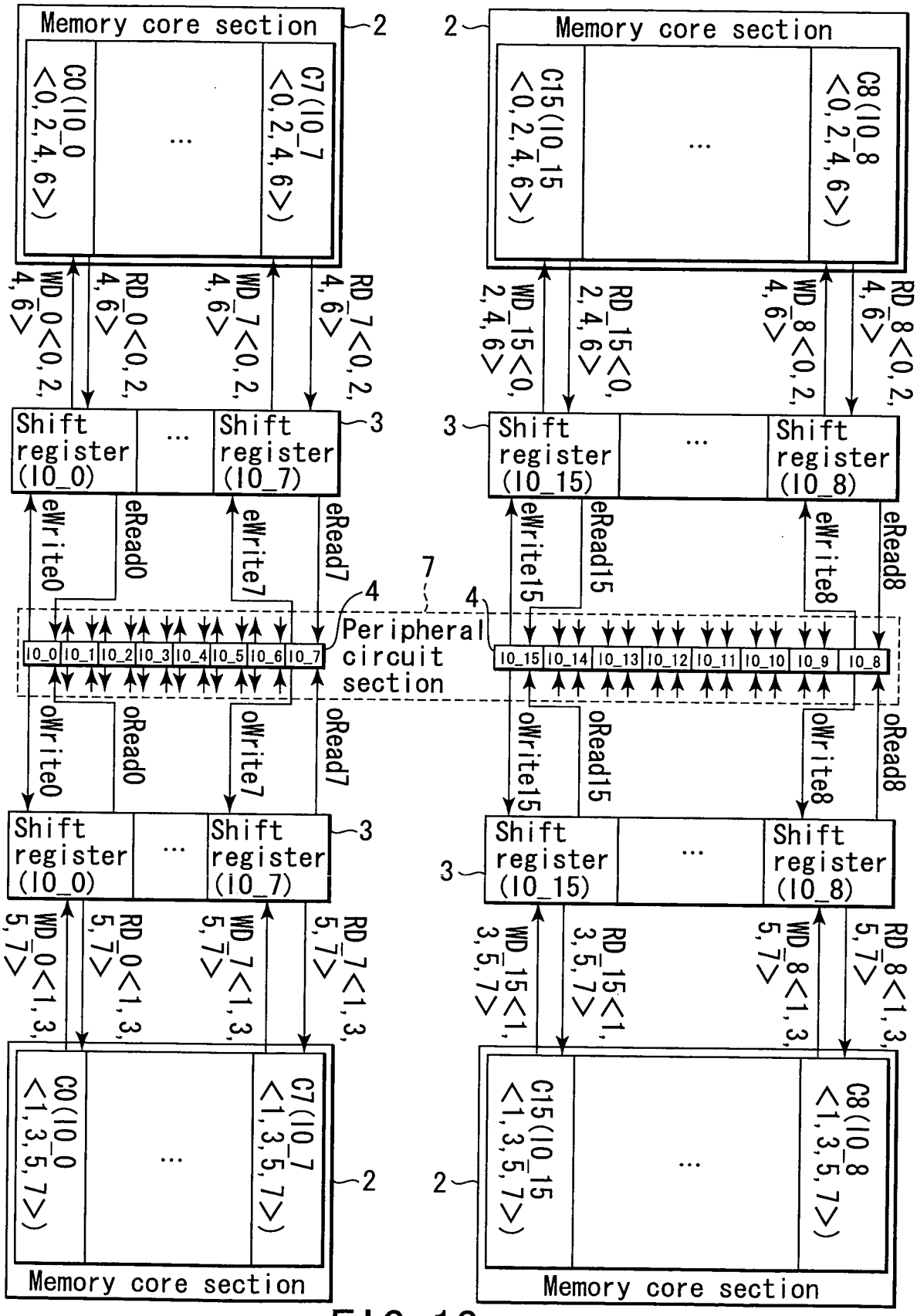

Memory core section
2
C0(IO_0 <0,2,4,6>)
C7(IO_7 <0,2,4,6>)
C15(IO_15 <0,2,4,6>)
C8(IO_8 <0,2,4,6>)
WD_0<0,2,4,6>
RD_0<0,2,4,6>
WD_7<0,2,4,6>
RD_7<0,2,4,6>
WD_15<0,2,4,6>
RD_15<0,2,4,6>
WD_8<0,2,4,6>
RD_8<0,2,4,6>
Shift register (IO_0)
Shift register (IO_7)
Shift register (IO_15)
Shift register (IO_8)
3
eWrite0
eRead0
eWrite7
eRead7
eWrite15
eRead15
eWrite8
eRead8
7
4
Peripheral circuit section
IO_0 IO_1 IO_2 IO_3 IO_4 IO_5 IO_6 IO_7
IO_15 IO_14 IO_13 IO_12 IO_11 IO_10 IO_9 IO_8
oWrite0
oRead0
oWrite7
oRead7
oWrite15
oRead15
oWrite8
oRead8
WD_0<1,3,5,7>
RD_0<1,3,5,7>
WD_7<1,3,5,7>
RD_7<1,3,5,7>
WD_15<1,3,5,7>
RD_15<1,3,5,7>
WD_8<1,3,5,7>
RD_8<1,3,5,7>
C0(IO_0 <1,3,5,7>)
C7(IO_7 <1,3,5,7>)
C15(IO_15 <1,3,5,7>)
C8(IO_8 <1,3,5,7>)
Memory core section

FIG. 18

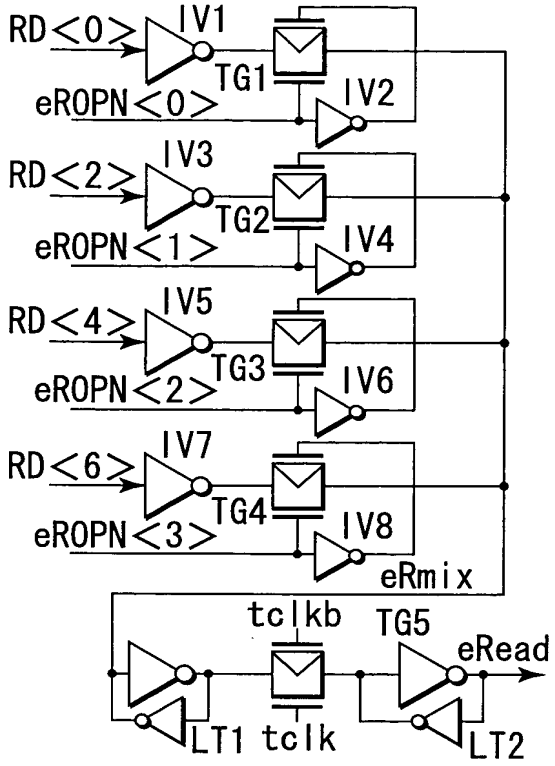


FIG. 19A

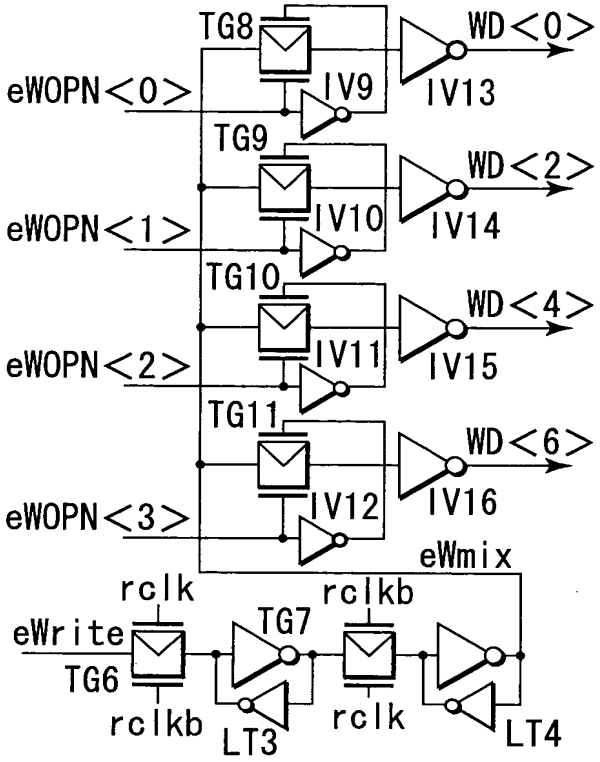


FIG. 19B

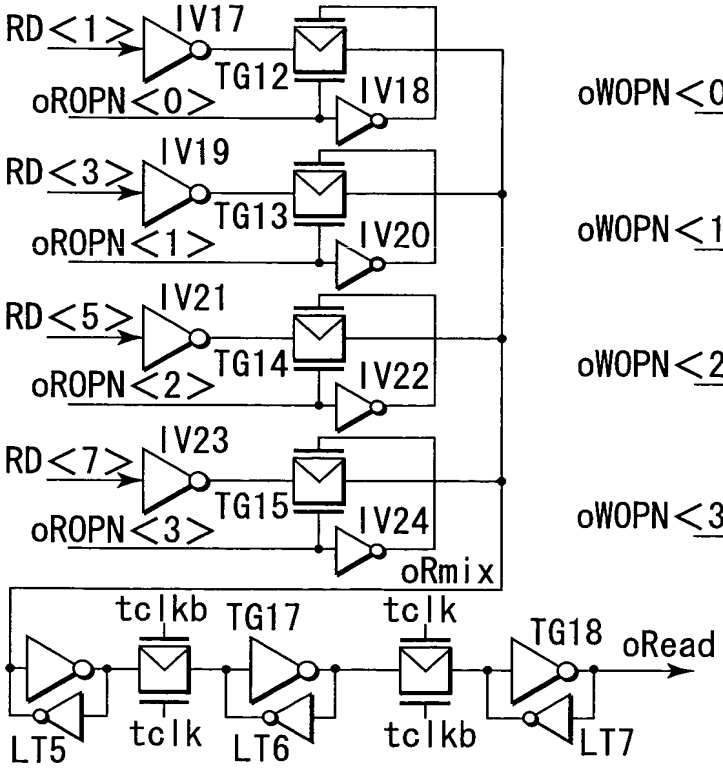


FIG. 20A

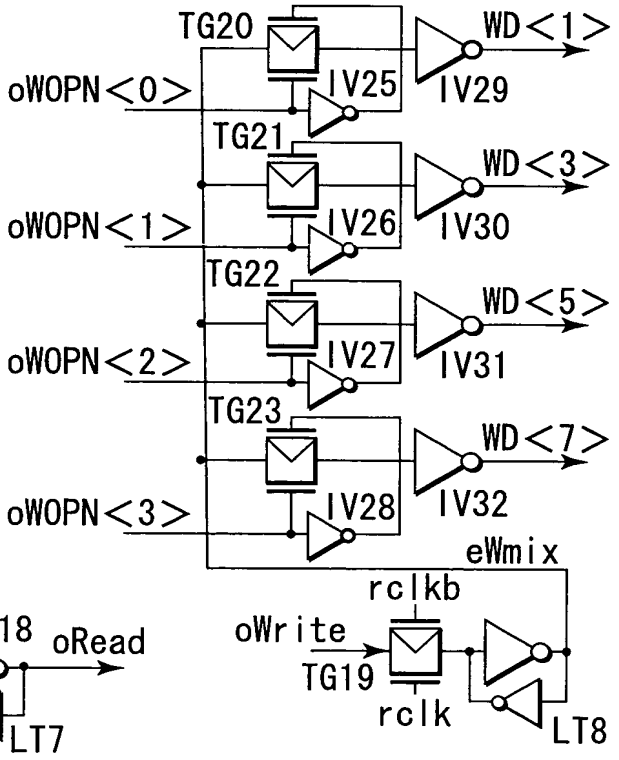


FIG. 20B

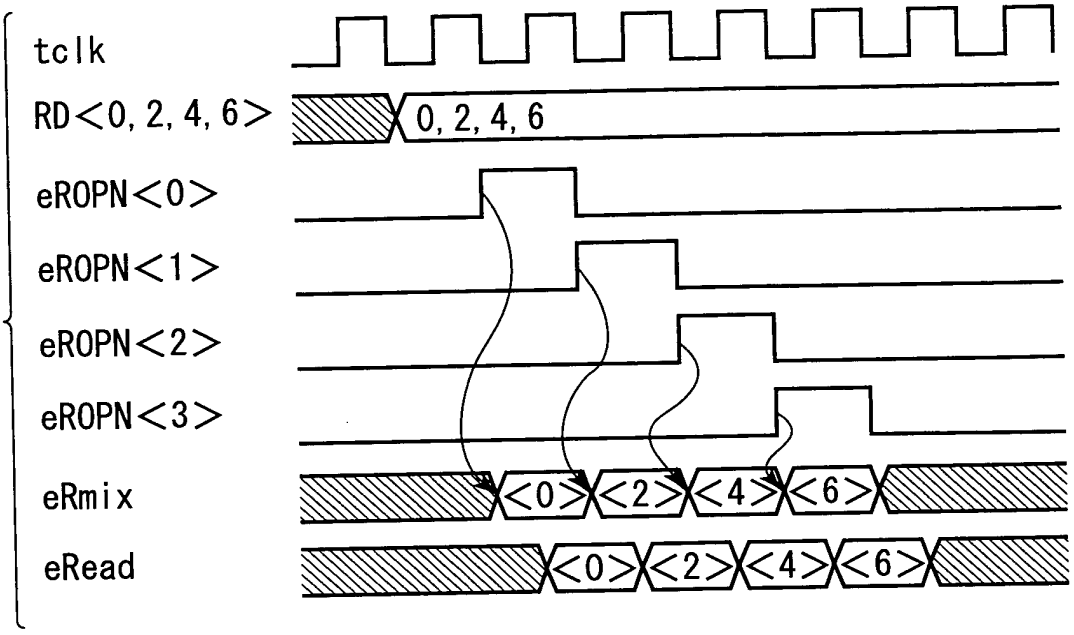

tclk
RD<0, 2, 4, 6>
0, 2, 4, 6
eROPN<0>
eROPN<1>
eROPN<2>
eROPN<3>
eRmix
eRead
<0>
<2>
<4>
<6>
<0>
<2>
<4>
<6>

FIG. 21

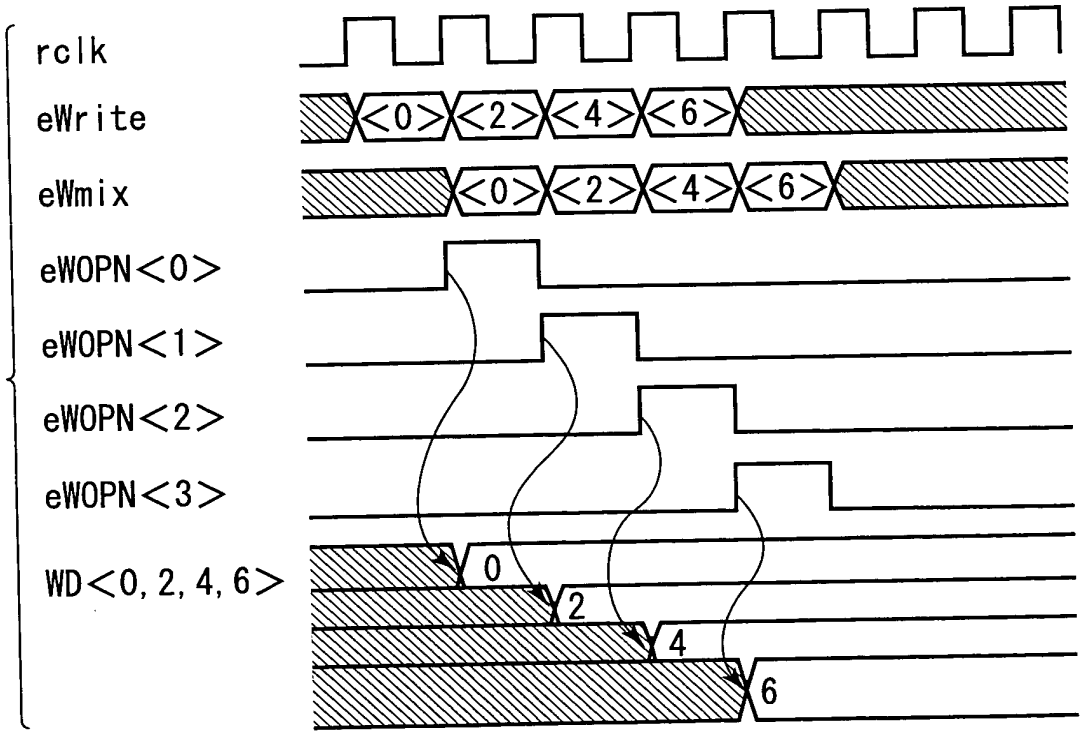

rclk
eWrite
eWmix
eWOPN<0>
eWOPN<1>
eWOPN<2>
eWOPN<3>
WD<0, 2, 4, 6>
<0>
<2>
<4>
<6>
<0>
<2>
<4>
<6>
0
2
4
6

FIG. 22

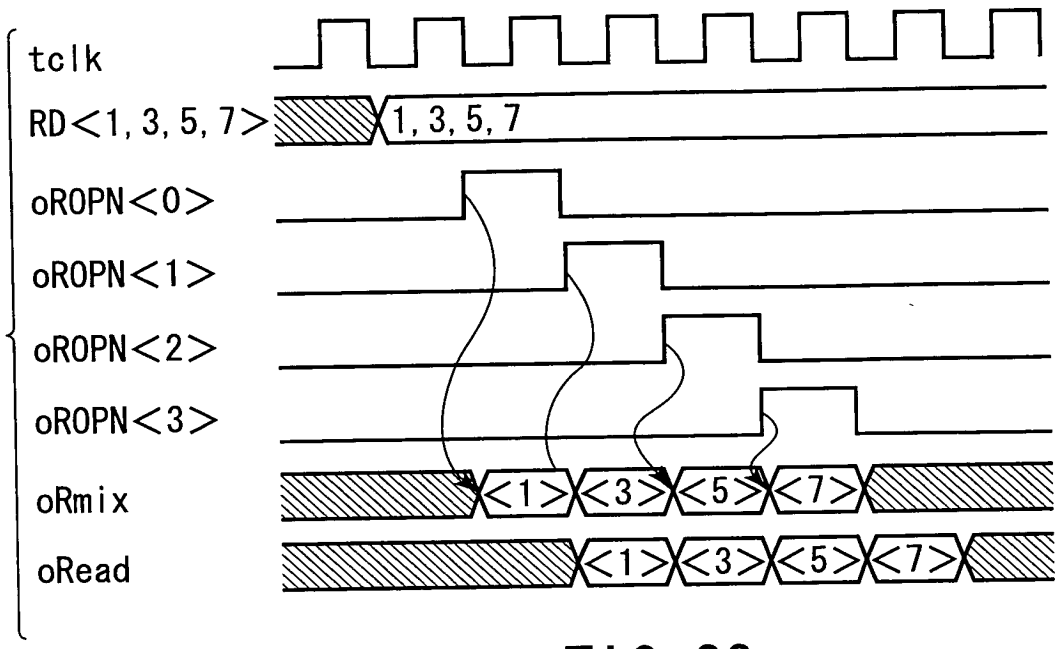

tclk
RD<1, 3, 5, 7>
1, 3, 5, 7
oROPN<0>
oROPN<1>
oROPN<2>
oROPN<3>
oRmix
oRead
<1>
<3>
<5>
<7>

FIG. 23

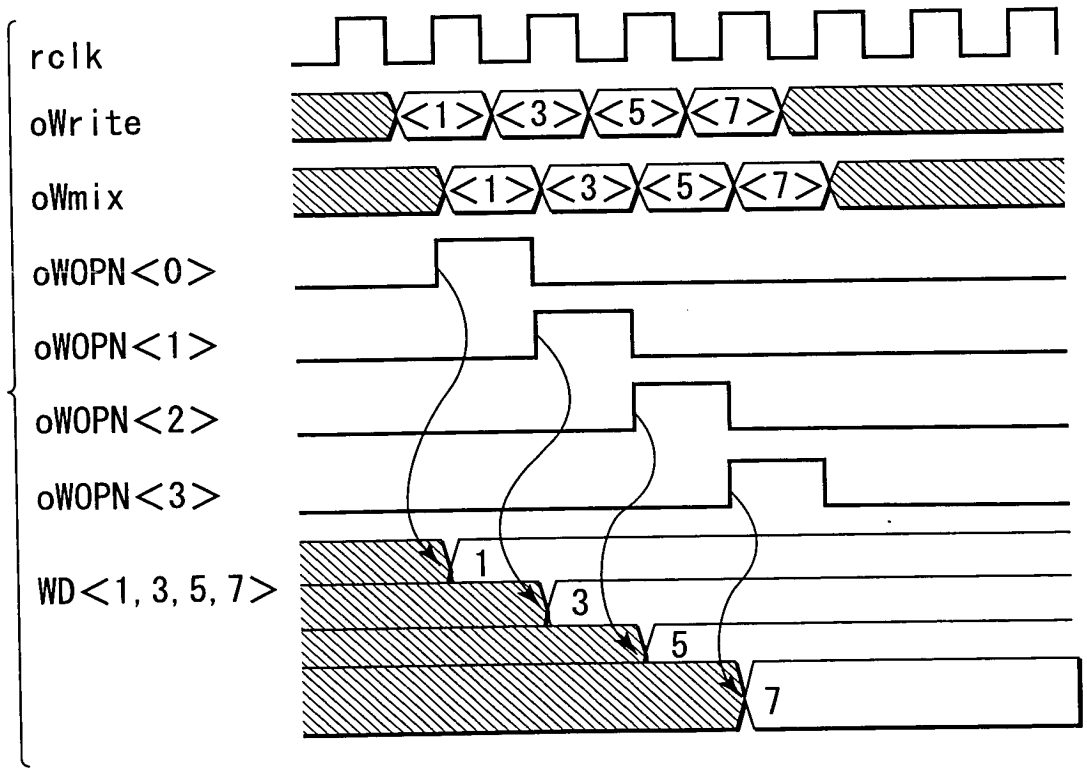

rclk
oWrite
oWmix
oWOPN<0>
oWOPN<1>
oWOPN<2>
oWOPN<3>
WD<1, 3, 5, 7>
<1>
<3>
<5>
<7>
1
3
5
7

FIG. 24

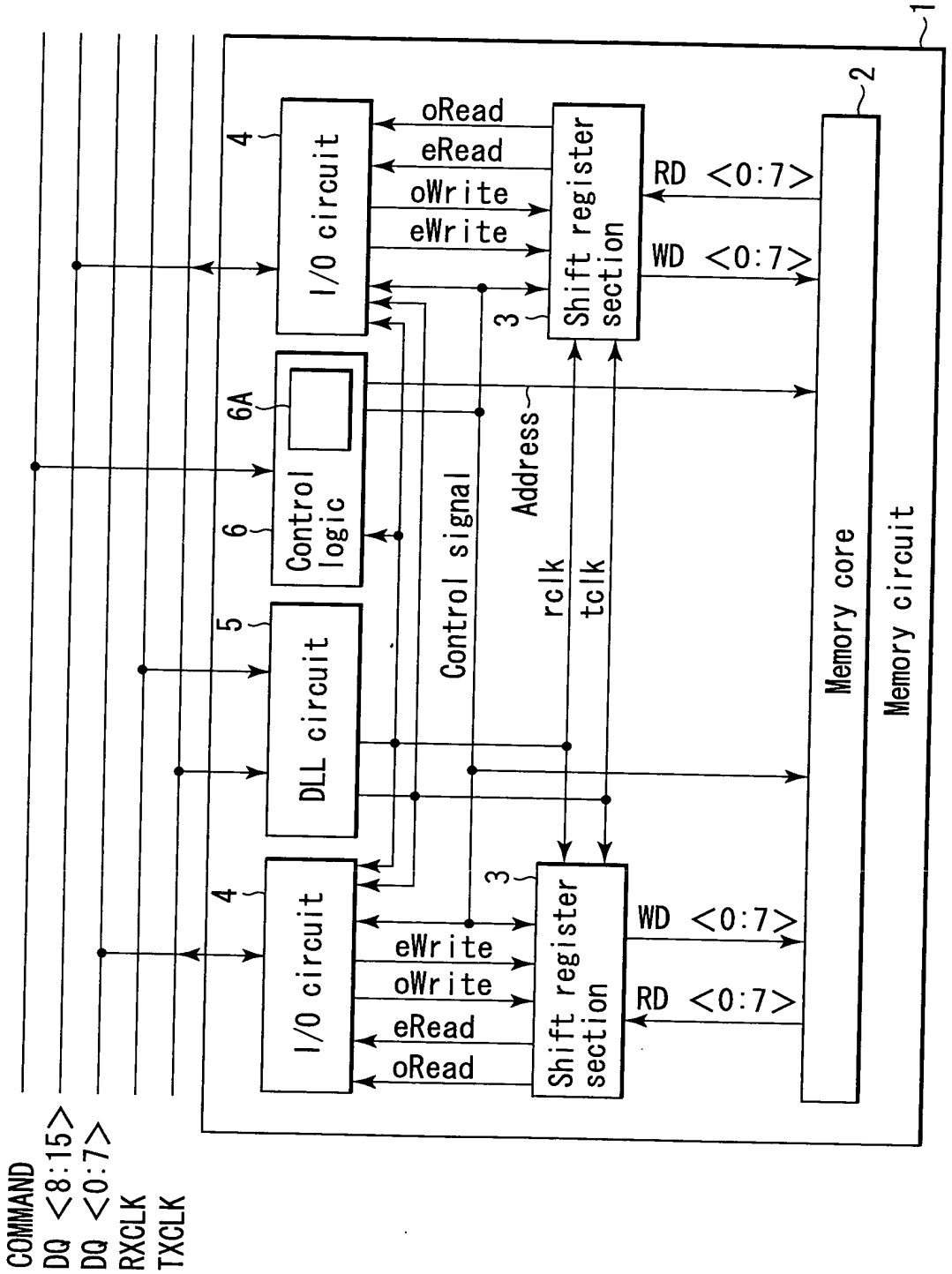

COMMAND
DQ <8:15>
DQ <0:7>
RXCLK
TXCLK
1
2
Memory circuit
Memory core
I/O circuit
4
oRead
eRead
oWrite
eWrite
Shift register section
3
RD <0:7>
WD <0:7>
6A
Control logic
6
Address
Control signal
rclk
tclk
DLL circuit
5
I/O circuit
4
eWrite
oWrite
eRead
oRead
Shift register section
3
WD <0:7>
RD <0:7>

FIG. 25

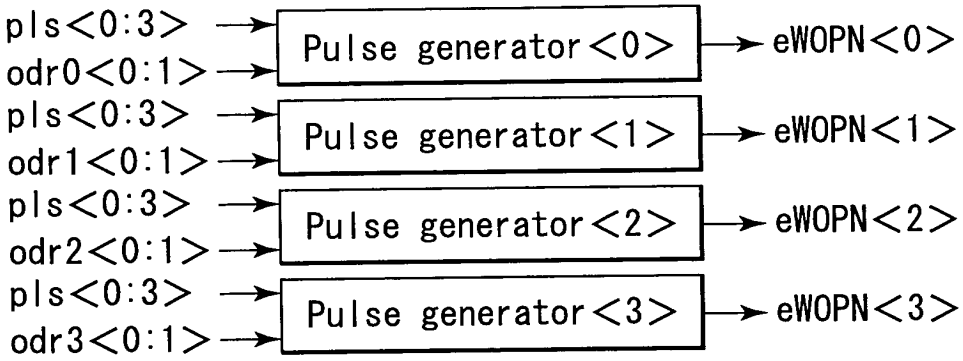


FIG. 26A

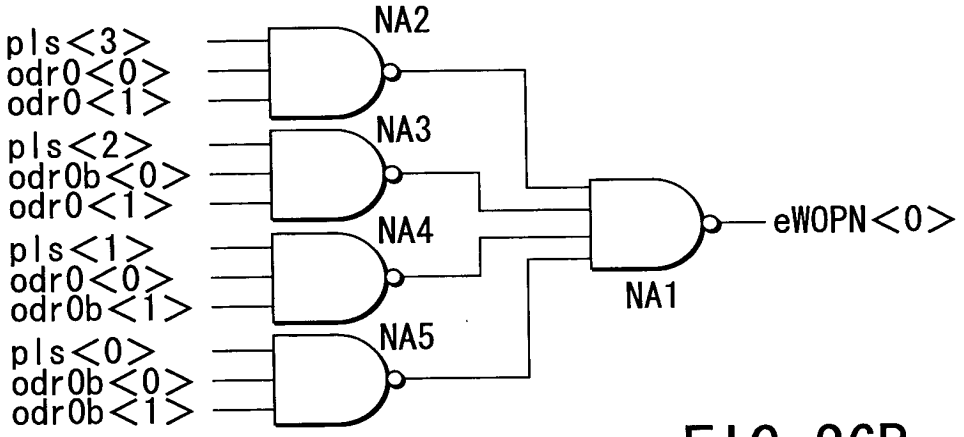


FIG. 26B

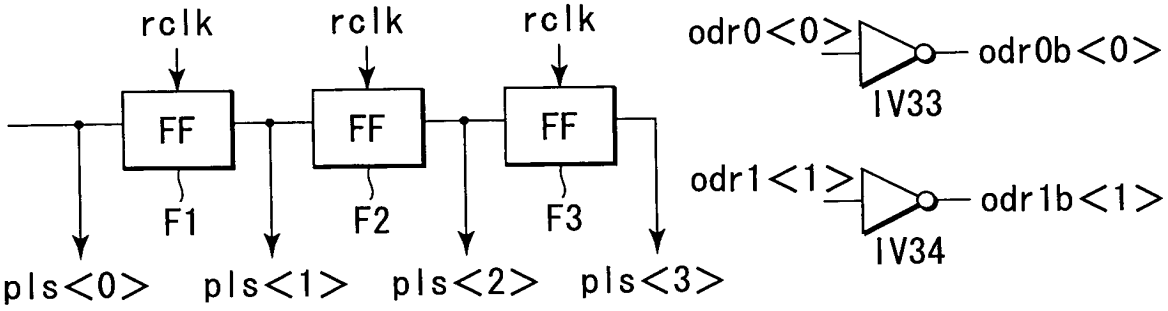


FIG. 26C

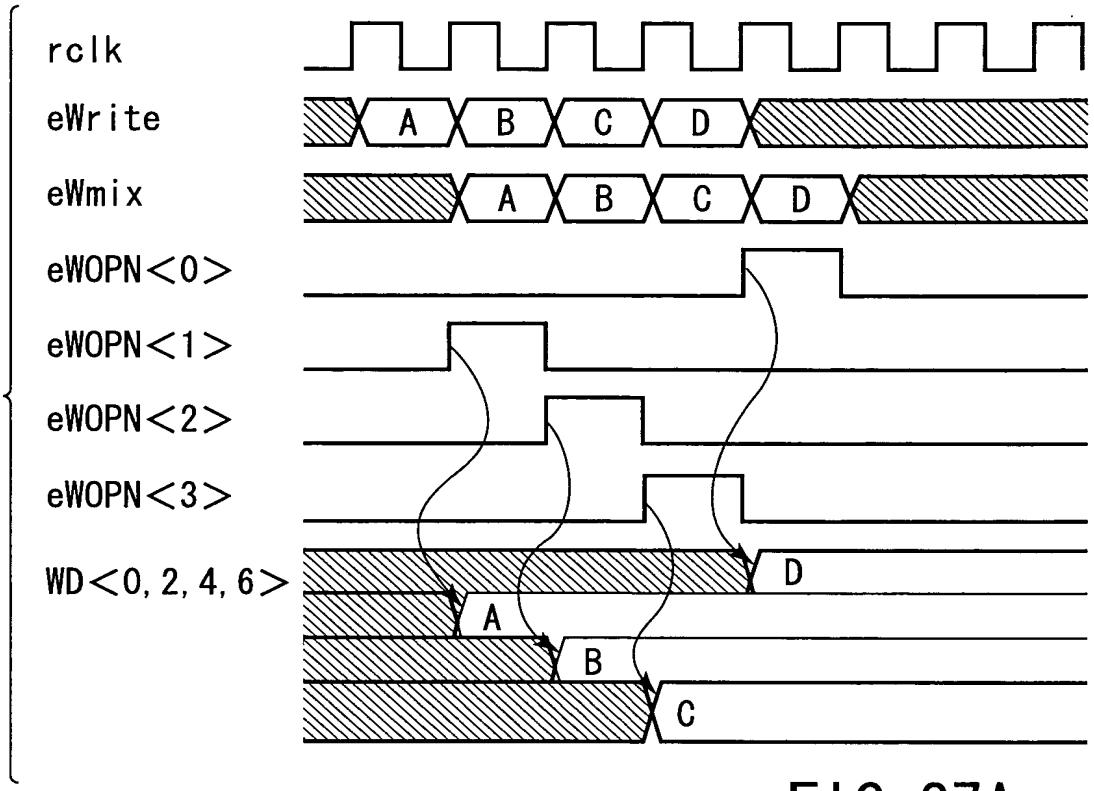


FIG. 27A

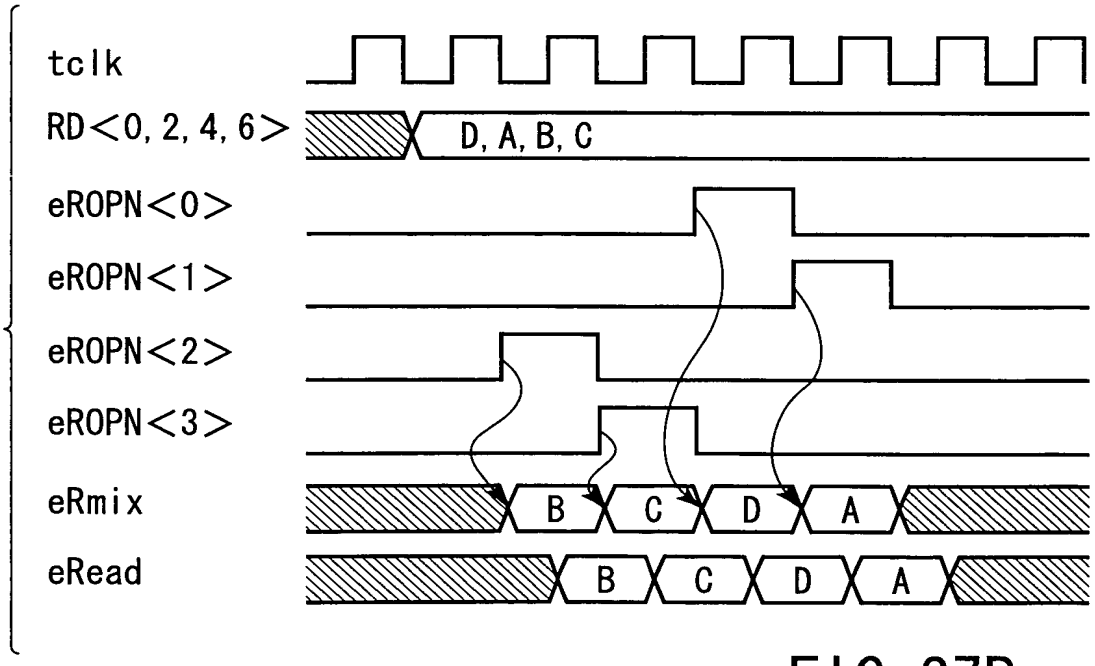
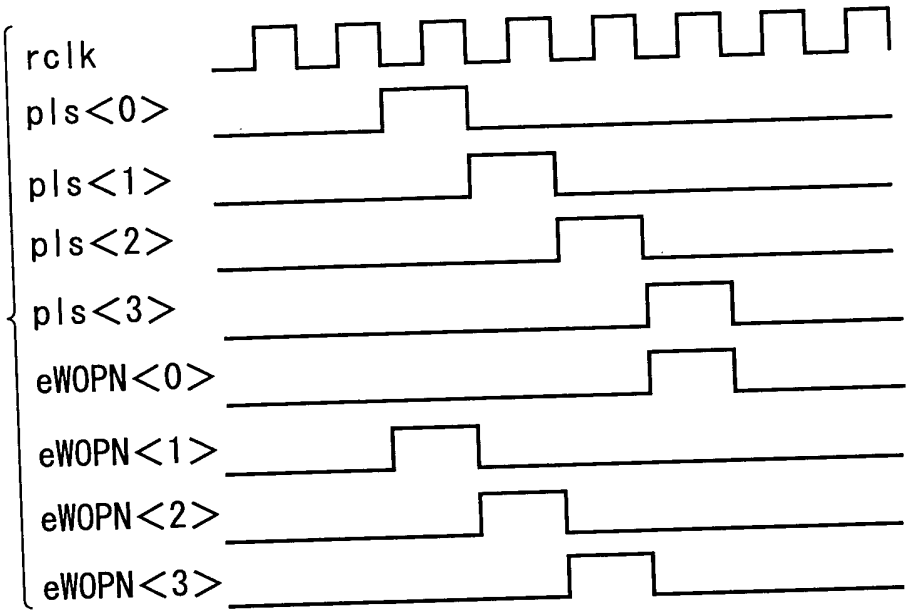


FIG. 27B

FIG. 28B



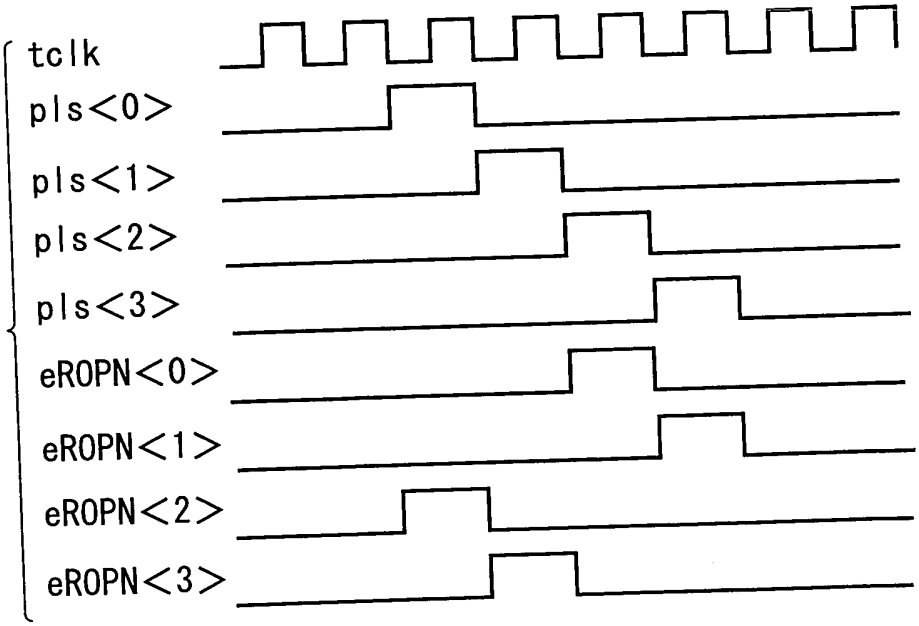
	<1>	<0>
odr0<0:1>	H	H
odr1<0:1>	L	L
odr2<0:1>	L	H
odr3<0:1>	H	L

FIG. 28A

	<1>	<0>
odr0<0:1>	H	L
odr1<0:1>	H	H
odr2<0:1>	L	L
odr3<0:1>	L	H

FIG. 29A

FIG. 29B



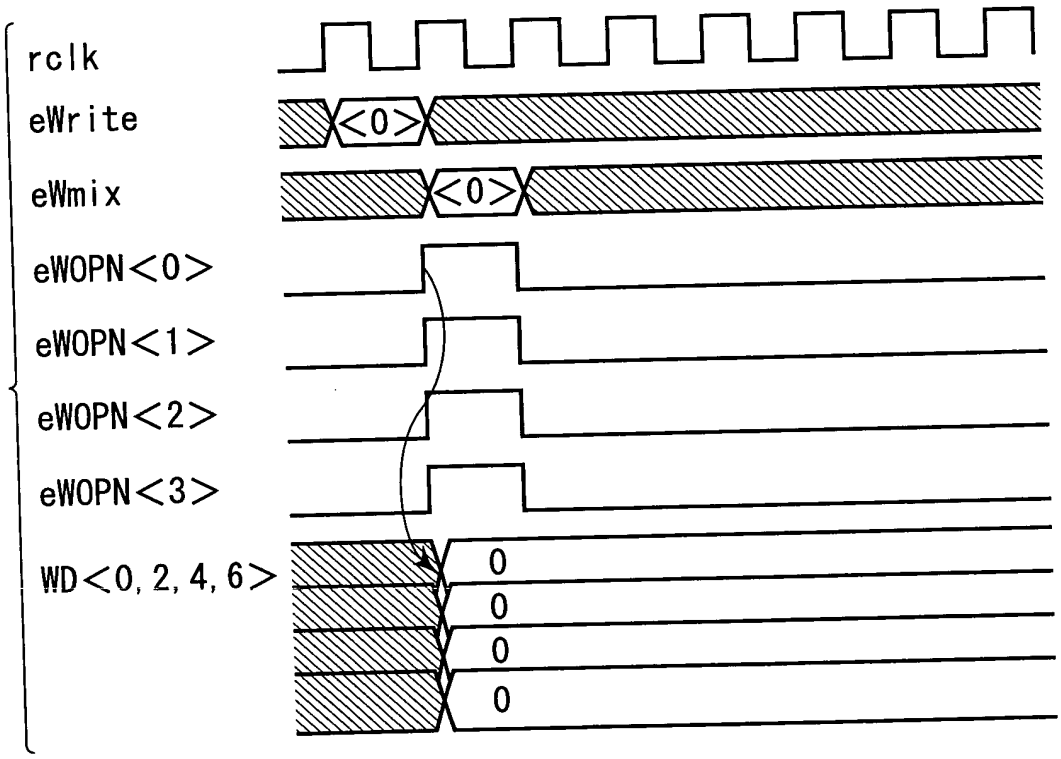
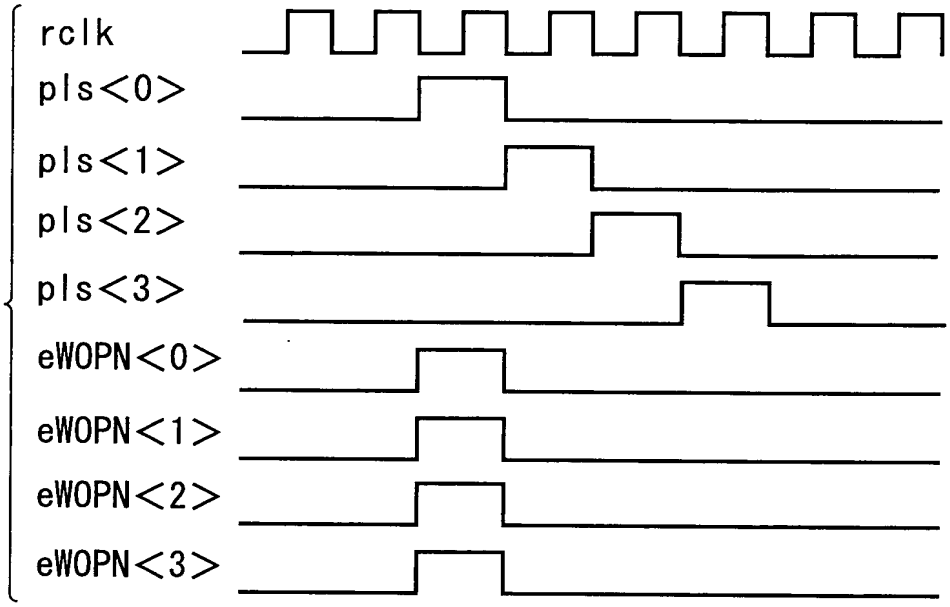

rclk
eWrite
<0>
eWmix
<0>
eWOPN<0>
eWOPN<1>
eWOPN<2>
eWOPN<3>
WD<0, 2, 4, 6>
0
0
0
0

FIG. 30

FIG. 31B



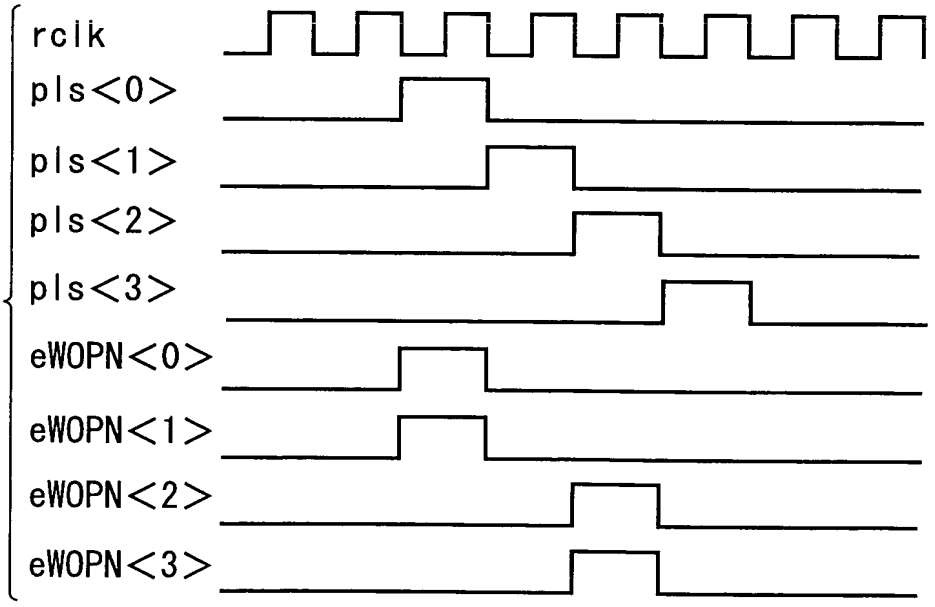
	<1>	<0>
odr0<0:1>	L	L
odr1<0:1>	L	L
odr2<0:1>	L	L
odr3<0:1>	L	L

FIG. 31A

	<1>	<0>
odr0<0:1>	L	L
odr1<0:1>	L	L
odr2<0:1>	H	L
odr3<0:1>	H	L

FIG. 32A

FIG. 32B



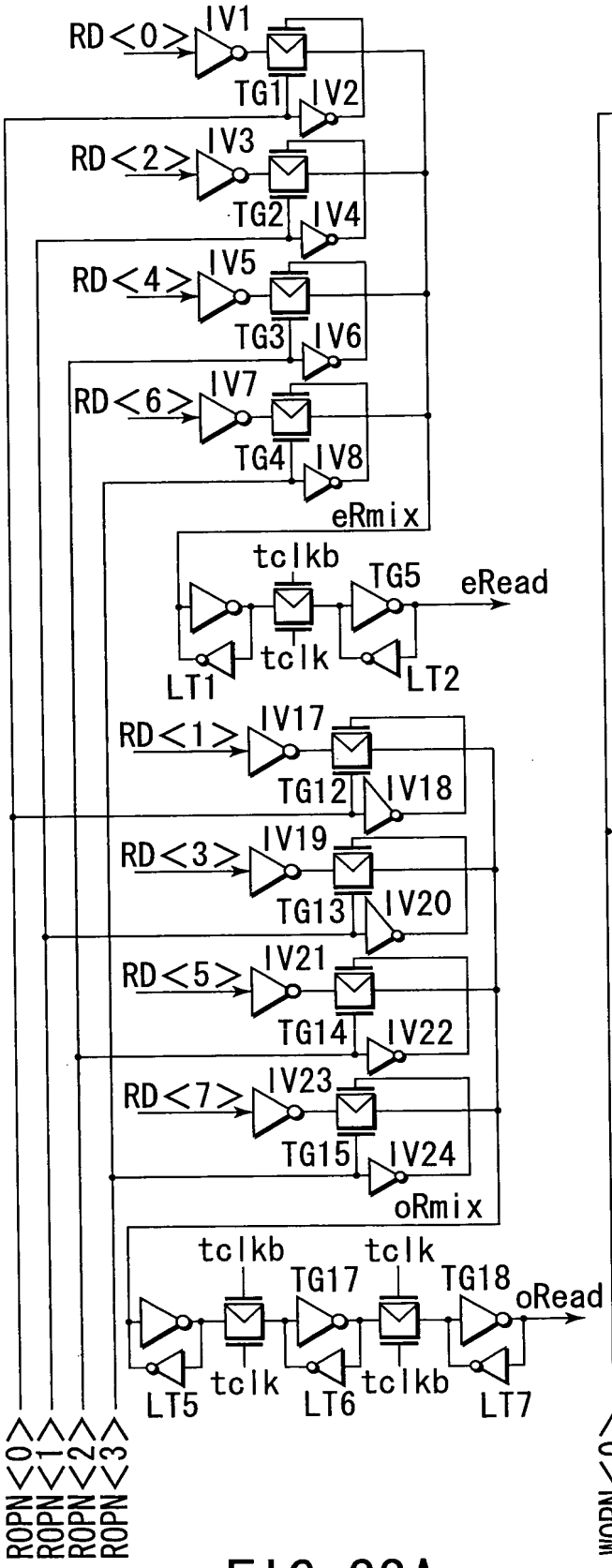


FIG. 33A

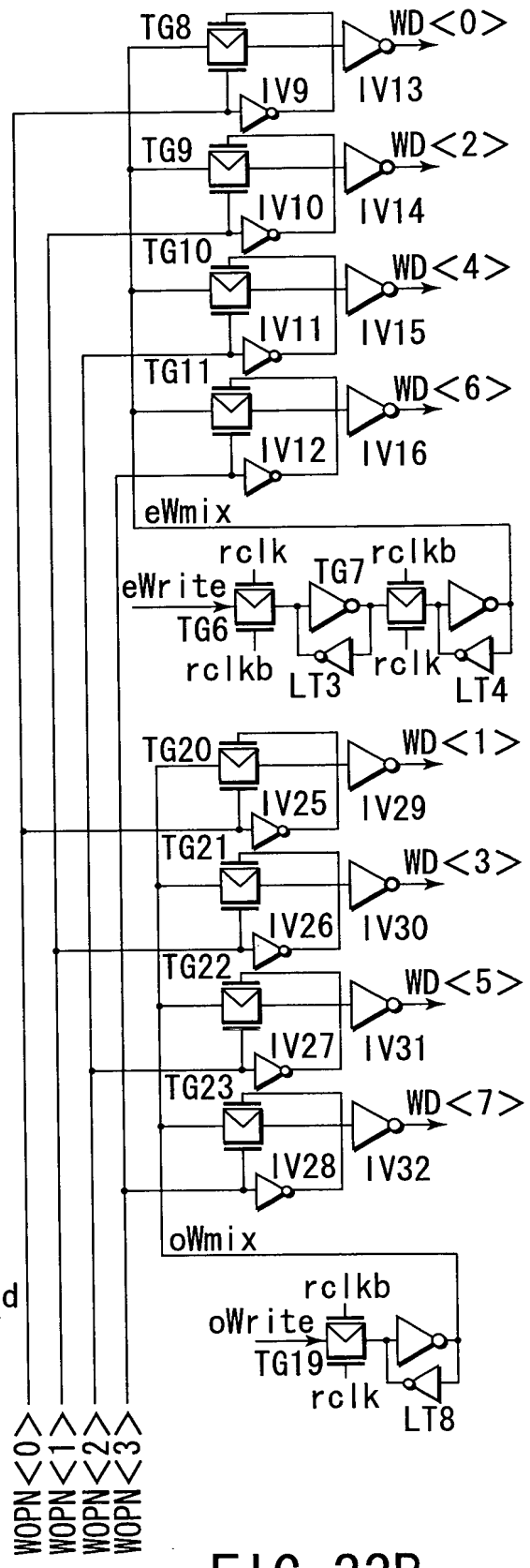


FIG. 33B

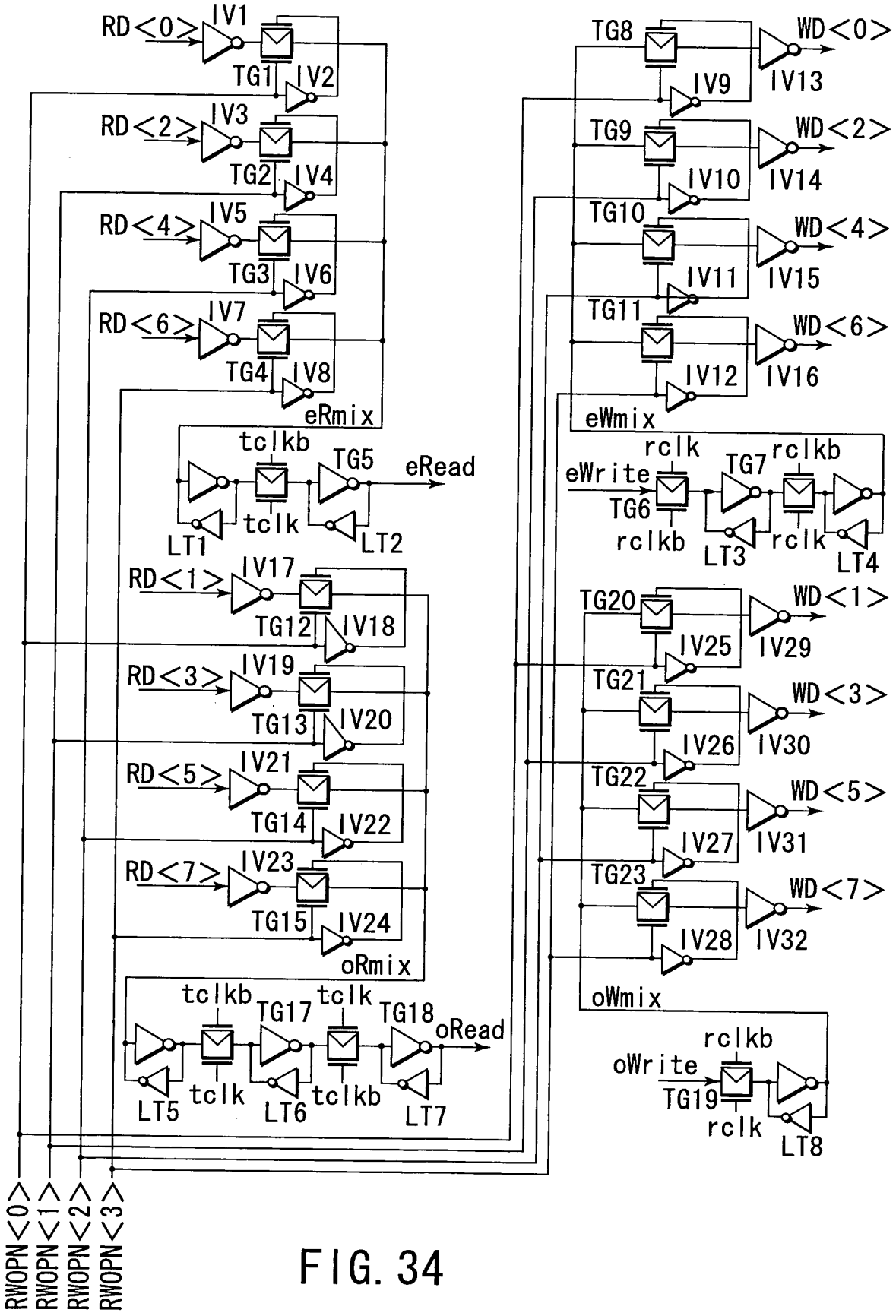

RD<0>
IV1
TG1
IV2
RD<2>
IV3
TG2
IV4
RD<4>
IV5
TG3
IV6
RD<6>
IV7
TG4
IV8
eRmix
tclkb
TG5
eRead
tclk
LT1
LT2
RD<1>
IV17
TG12
IV18
RD<3>
IV19
TG13
IV20
RD<5>
IV21
TG14
IV22
RD<7>
IV23
TG15
IV24
oRmix
tclkb
TG17
tclk
TG18
oRead
LT5
tclk
LT6
tclkb
LT7
RWOPN<0>
RWOPN<1>
RWOPN<2>
RWOPN<3>
TG8
IV9
WD<0>
IV13
TG9
IV10
WD<2>
IV14
TG10
IV11
WD<4>
IV15
TG11
IV12
WD<6>
IV16
eWmix
rclk
eWrite
TG6
rclkb
TG7
rclkb
LT3
rclk
LT4
TG20
IV25
WD<1>
IV29
TG21
IV26
WD<3>
IV30
TG22
IV27
WD<5>
IV31
TG23
IV28
WD<7>
IV32
oWmix
rclkb
oWrite
TG19
rclk
LT8

FIG. 34